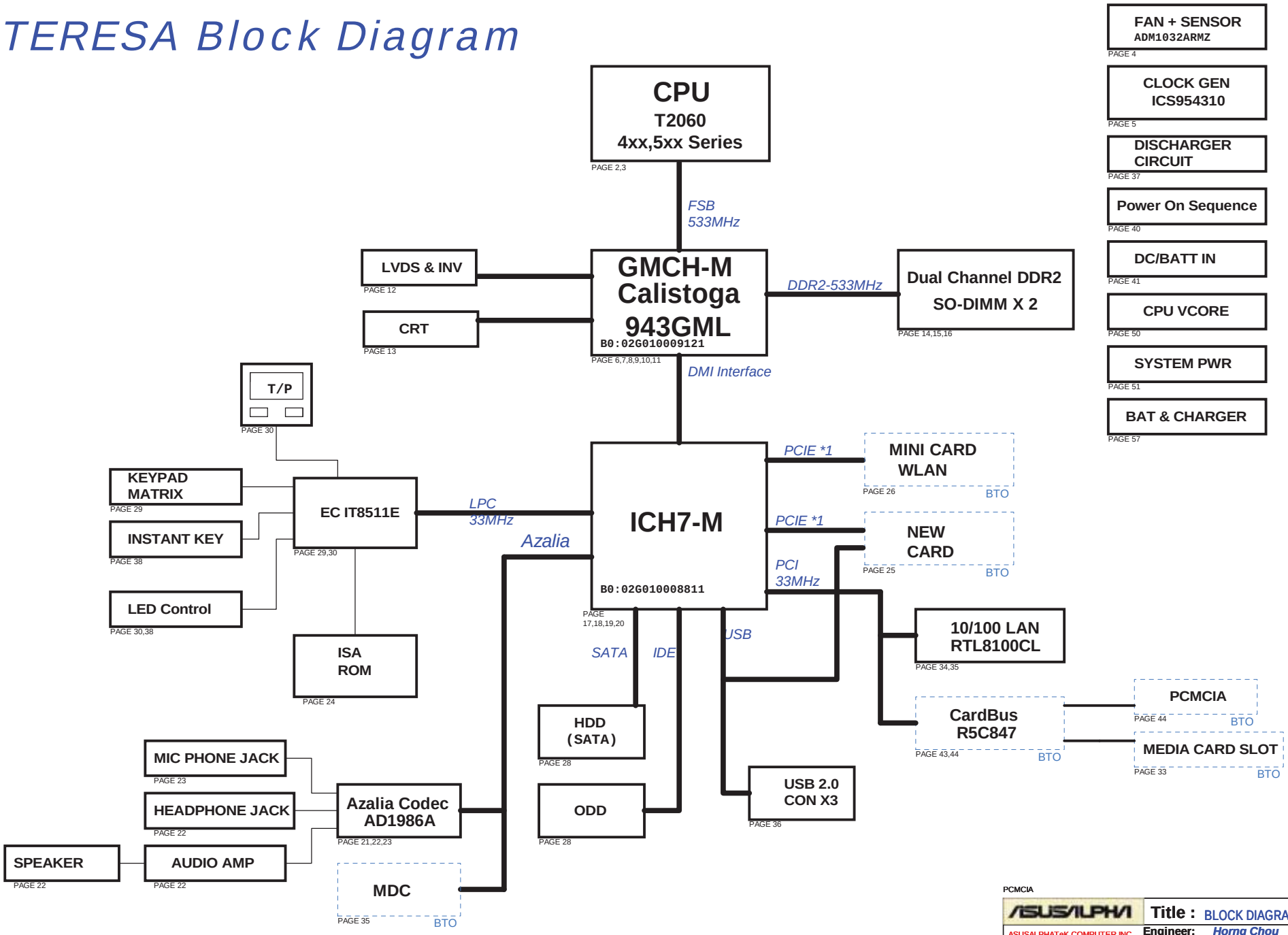
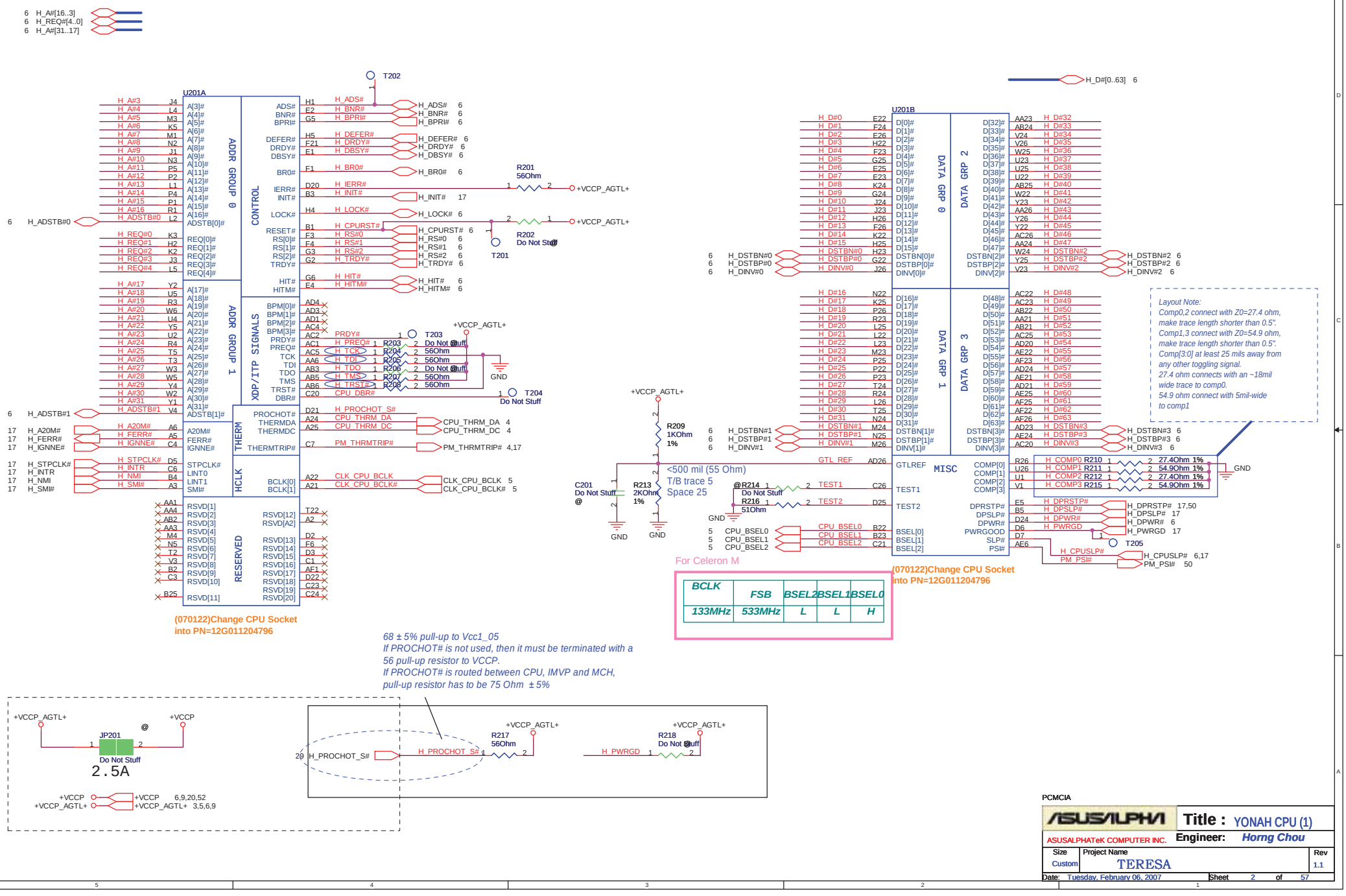
TERESA Block Diagram



PCMCIA

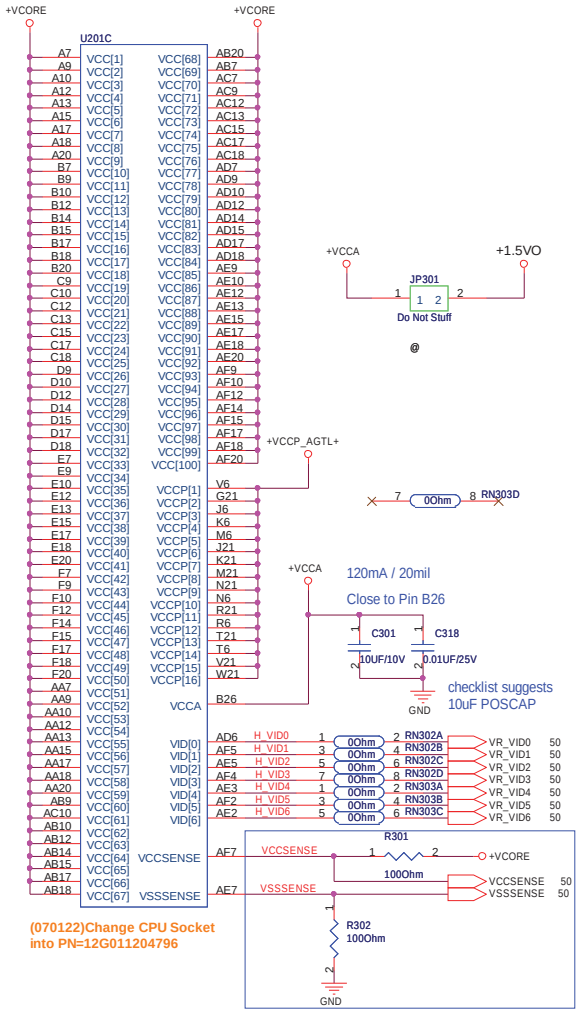
ASUSALPHA	Title : BLOCK DIAGRAM	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 1 of 57	



Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCC	1.0V	1.2V	1.3V
	C3	C2	C0
ICC	14.7A	16.5A	29Ah

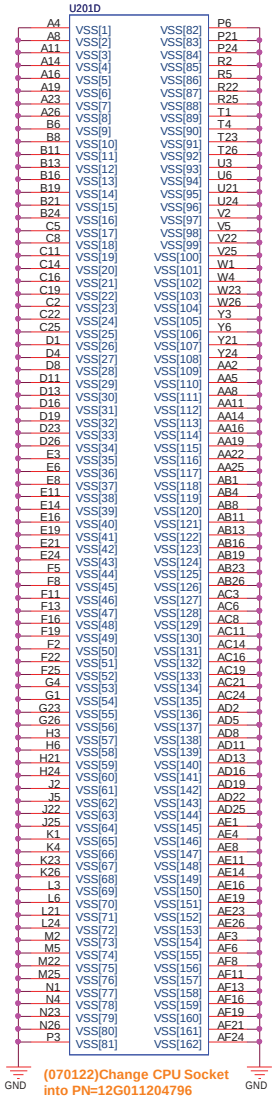
Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
	MIN	TYP	MAX
ICCP			2.5A

Modity Table for Celeron M

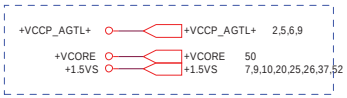


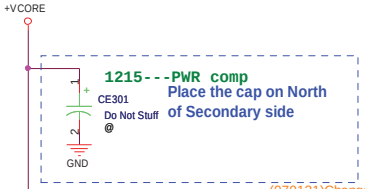
(070122)Change CPU Socket into PN=12G011204796

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.



(070122)Change CPU Socket into PN=12G011204796

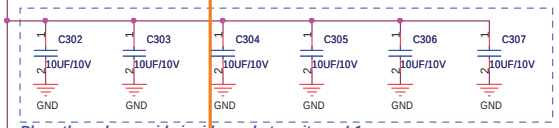




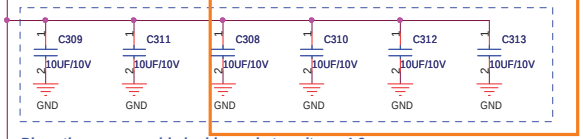
Vcc Core Decoupling Caps
Primary side => Bottom side
Secondary side => Top side

(070131)Change 22UF into 10UF

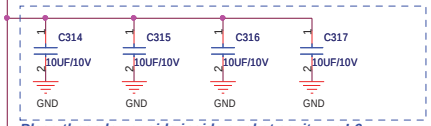
Place these upper side inside socket cavity on L1



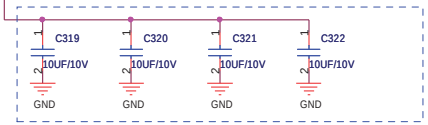
Place these lower side inside socket cavity on L1



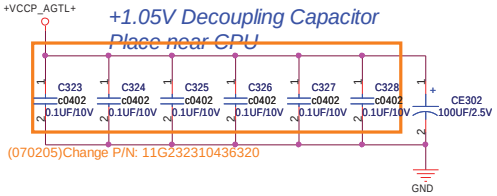
Place these upper side inside socket cavity on L6



Place these lower side inside socket cavity on L6



(061228)Change into 10UF/10V PN:11G236322636360
C302,C303,C309,C311
C314,C315,C316,C317
C319,C320,C321,C322

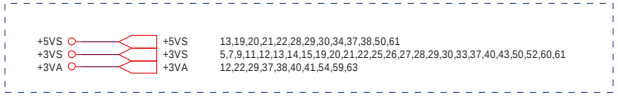


(070205)Change P/N: 11G232310436320

PCMCIA

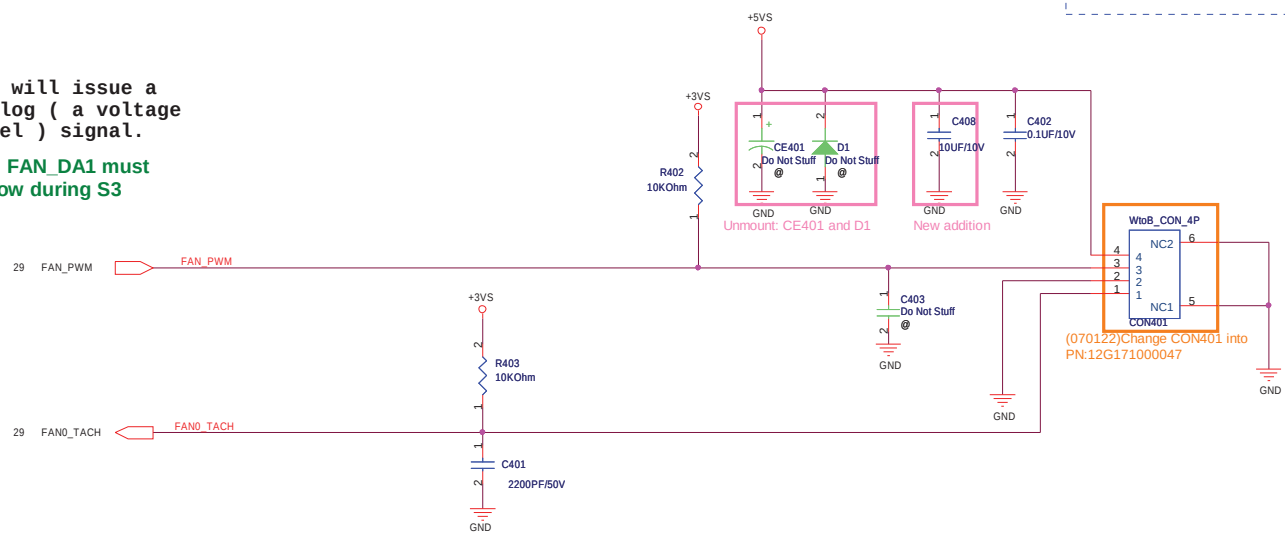
ASUSALPHA	Title :	Yonah CPU (2)
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 3 of 57	

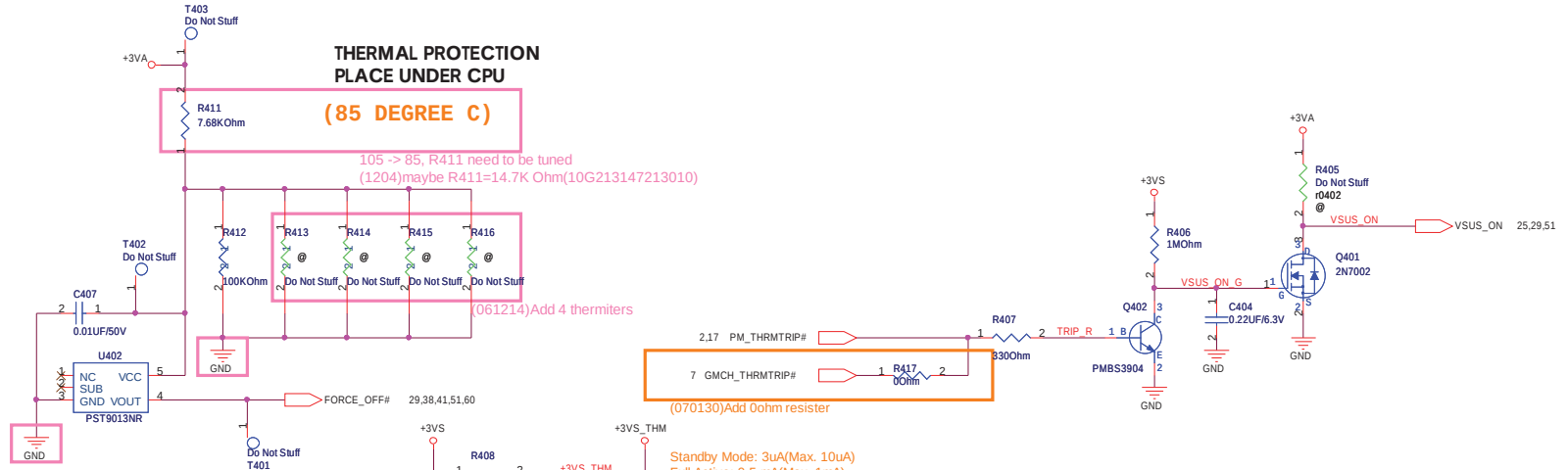
Fan Speed Control



KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3





Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

ASUSALPHA

Title : THER-SENSOR,FAN

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 4 of 57

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,6,9

+3VS → +3VS 4,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

(070130)Change C516 from 27PF to 33PF

Delete CLK_ITPMPCI(connect to pin37)

(070205) R533 Remove

Remove 0ohm

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Realtek:Mount R519,Remove R550 R534

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

Internal Pull-Up Resistor

Internal Pull-Down Resistor

PCMCIA

ASUSALPHA | Title : CLOCK GEN

ASUSALPHATeK COMPUTER INC. | Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 5 of 57

2 H_D#[0..63]

H_A#[31..3] 2

+VCCP 2,9,20,52

+VCCP_AGTL+ 2,3,5,9

U601A

HOST

H_D#0	F1	H_D#_0	
H_D#1	J1	H_D#_1	
H_D#2	H1	H_D#_2	
H_D#3	J6	H_D#_3	
H_D#4	H3	H_D#_4	
H_D#5	K2	H_D#_5	
H_D#6	G1	H_D#_6	
H_D#7	G2	H_D#_7	
H_D#8	K9	H_D#_8	
H_D#9	K1	H_D#_9	
H_D#10	K7	H_D#_10	
H_D#11	J8	H_D#_11	
H_D#12	H4	H_D#_12	
H_D#13	J3	H_D#_13	
H_D#14	K11	H_D#_14	
H_D#15	G4	H_D#_15	
H_D#16	T10	H_D#_16	
H_D#17	W11	H_D#_17	
H_D#18	T3	H_D#_18	
H_D#19	U7	H_D#_19	
H_D#20	U9	H_D#_20	
H_D#21	U11	H_D#_21	
H_D#22	T11	H_D#_22	
H_D#23	W9	H_D#_23	
H_D#24	T1	H_D#_24	
H_D#25	T8	H_D#_25	
H_D#26	T4	H_D#_26	
H_D#27	W7	H_D#_27	
H_D#28	U5	H_D#_28	
H_D#29	T9	H_D#_29	
H_D#30	W6	H_D#_30	
H_D#31	T5	H_D#_31	
H_D#32	AB7	H_D#_32	
H_D#33	AA9	H_D#_33	
H_D#34	W4	H_D#_34	
H_D#35	W3	H_D#_35	
H_D#36	Y3	H_D#_36	
H_D#37	Y7	H_D#_37	
H_D#38	W5	H_D#_38	
H_D#39	Y10	H_D#_39	
H_D#40	AB8	H_D#_40	
H_D#41	W2	H_D#_41	
H_D#42	AA4	H_D#_42	
H_D#43	AA7	H_D#_43	
H_D#44	AA2	H_D#_44	
H_D#45	AA6	H_D#_45	
H_D#46	AA10	H_D#_46	
H_D#47	Y8	H_D#_47	
H_D#48	AA1	H_D#_48	
H_D#49	AB4	H_D#_49	
H_D#50	AC9	H_D#_50	
H_D#51	AB11	H_D#_51	
H_D#52	AC11	H_D#_52	
H_D#53	AB3	H_D#_53	
H_D#54	AC2	H_D#_54	
H_D#55	AD1	H_D#_55	
H_D#56	AD9	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AD7	H_D#_58	
H_D#59	AC6	H_D#_59	
H_D#60	AB5	H_D#_60	
H_D#61	AD10	H_D#_61	
H_D#62	AD4	H_D#_62	
H_D#63	AC8	H_D#_63	

H_XRCOMP	E1	H_XRCOMP	
H_XSCOMP	E2	H_XSCOMP	
H_XSWING	E4	H_XSWING	
H_YRCOMP	Y1	H_YRCOMP	
H_YSCOMP	U1	H_YSCOMP	
H_YSWING	W1	H_YSWING	
5 CLK_MCH_BCLK	AG2	H_CLKIN	
5 CLK_MCH_BCLK#	AG1	H_CLKIN#	

H_A#_3	H9	H_A#3	
H_A#_4	C9	H_A#4	
H_A#_5	E11	H_A#5	
H_A#_6	G11	H_A#6	
H_A#_7	F11	H_A#7	
H_A#_8	G12	H_A#8	
H_A#_9	F9	H_A#9	
H_A#_10	H11	H_A#10	
H_A#_11	J12	H_A#11	
H_A#_12	G14	H_A#12	
H_A#_13	D9	H_A#13	
H_A#_14	J14	H_A#14	
H_A#_15	H13	H_A#15	
H_A#_16	J15	H_A#16	
H_A#_17	F14	H_A#17	
H_A#_18	D12	H_A#18	
H_A#_19	A11	H_A#19	
H_A#_20	C11	H_A#20	
H_A#_21	A12	H_A#21	
H_A#_22	A13	H_A#22	
H_A#_23	E13	H_A#23	
H_A#_24	G13	H_A#24	
H_A#_25	F12	H_A#25	
H_A#_26	B12	H_A#26	
H_A#_27	B14	H_A#27	
H_A#_28	C12	H_A#28	
H_A#_29	A14	H_A#29	
H_A#_30	C14	H_A#30	
H_A#_31	D14	H_A#31	

H_ADS#	E8	H_ADS#	H_ADS# 2
H_ADSTB#_0	B9	H_ADSTB#0	H_ADSTB#0 2
H_ADSTB#_1	C13	H_ADSTB#1	H_ADSTB#1 2
H_AVREF	J13	H_VREF	
H_BNR#	C6	H_BNR#	H_BNR# 2
H_BPRI#	F6	H_BPRI#	H_BPRI# 2
H_BREQ#0	C7	H_BR0#	H_BR0# 2
H_CPURST#	B7	H_CPURST#	H_CPURST# 2
H_DBSY#	A7	H_DBSY#	H_DBSY# 2
H_DEFER#	C3	H_DEFER#	H_DEFER# 2
H_DPWR#	J9	H_DPWR#	H_DPWR# 2
H_DRDY#	H8	H_DRDY#	H_DRDY# 2
H_DVREF	K13		

H_DINV#_0	J7	H_DINV#0	H_DINV#0 2
H_DINV#_1	W8	H_DINV#1	H_DINV#1 2
H_DINV#_2	U3	H_DINV#2	H_DINV#2 2
H_DINV#_3	AB10	H_DINV#3	H_DINV#3 2
H_DSTBN#_0	K4	H_DSTBN#0	H_DSTBN#0 2
H_DSTBN#_1	T7	H_DSTBN#1	H_DSTBN#1 2
H_DSTBN#_2	Y5	H_DSTBN#2	H_DSTBN#2 2
H_DSTBN#_3	AC4	H_DSTBN#3	H_DSTBN#3 2
H_DSTBP#_0	K3	H_DSTBP#0	H_DSTBP#0 2
H_DSTBP#_1	T6	H_DSTBP#1	H_DSTBP#1 2
H_DSTBP#_2	AA5	H_DSTBP#2	H_DSTBP#2 2
H_DSTBP#_3	AC5	H_DSTBP#3	H_DSTBP#3 2
H_HIT#	D3	H_HIT#	H_HIT# 2
H_HITM#	D4	H_HITM#	H_HITM# 2
H_LOCK#	B3	H_LOCK#	H_LOCK# 2
H_REQ#_0	D8	H_REQ#0	H_REQ#[4..0] 2
H_REQ#_1	G8	H_REQ#1	
H_REQ#_2	B8	H_REQ#2	
H_REQ#_3	F8	H_REQ#3	
H_REQ#_4	A8	H_REQ#4	
H_RS#_0	B4	H_RS#0	H_RS#[0..2] 2
H_RS#_1	E6	H_RS#1	
H_RS#_2	D6	H_RS#2	
H_SLPCPU#	E3	N_CPUSLP#	H_CPUSLP# 2,17
H_TRDY#	E7	H_TRDY#	H_TRDY# 2

CALISTOGA_Q137

+VCCP_AGTL+

R601 100Ohm 1%

R606 200Ohm 1%

C601 0.1UF/10V

GND

<500 mil (55 Ohm) T/B trace 5.5 , Space 25

Layout Note: 0.1uF should be placed 100mils or less from GMCH pin.

R611 0Ohm

N_CPUSLP# 2

+VCCP

R602 54.9Ohm 1%

R603 54.9Ohm 1%

5.5/20 mils

H_XSCOMP

H_YSCOMP

H_XRCOMP

H_YRCOMP

R604 24.9Ohm 1%

R605 24.9Ohm 1%

10/20mils

R607 221Ohm 1%

R608 100Ohm 1%

C602 0.1UF/10V

H_XSWING

10/20mils

R609 221Ohm 1%

R610 100Ohm 1%

C603 0.1UF/10V

H_YSWING

Signal voltage level = 0.3125*VCCP
Trace should be 10 mil wide with 20 mil spacing

PCMCIA

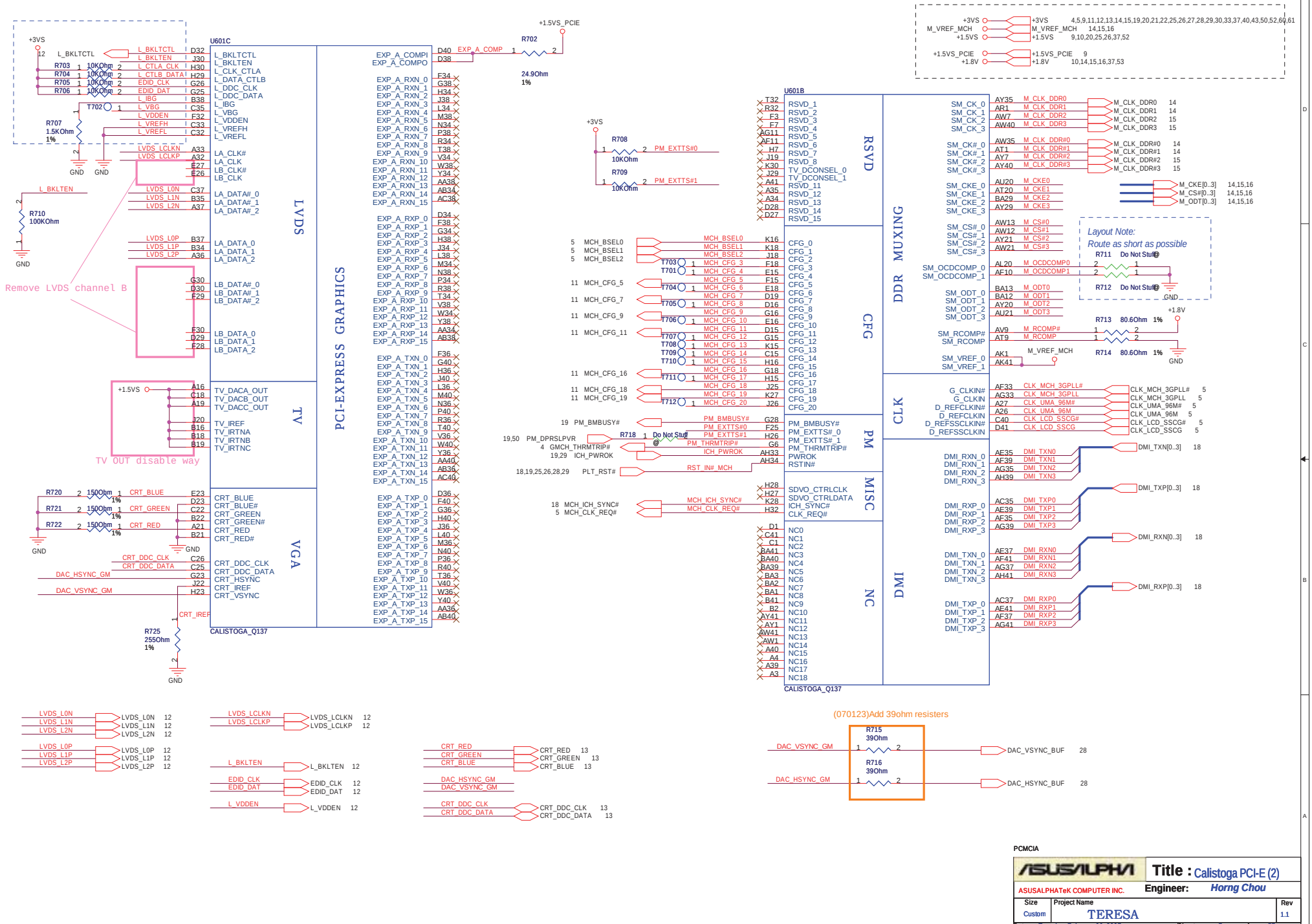
ASUSALPHA

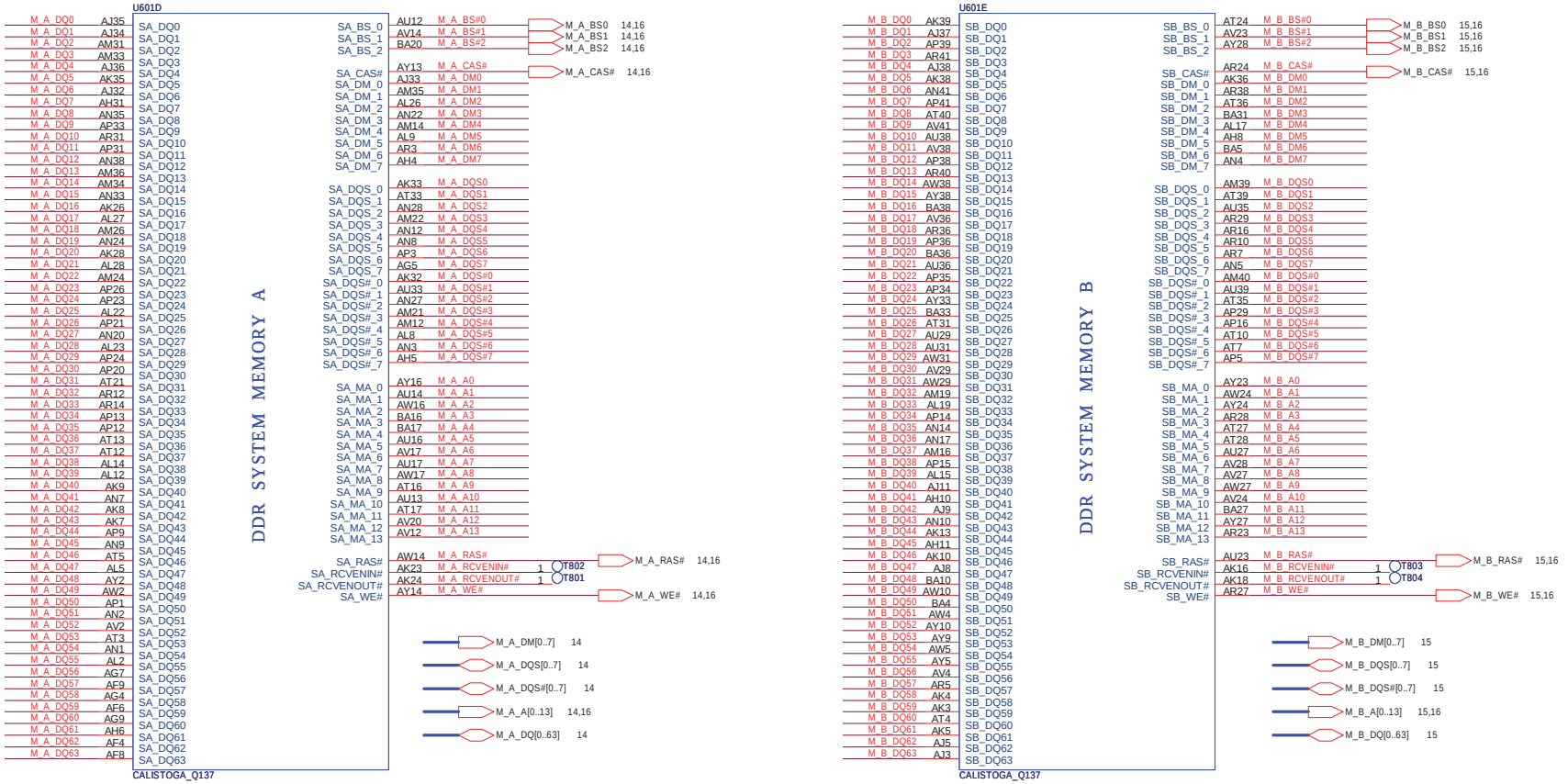
Title : Calistoga GMCH (1)

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

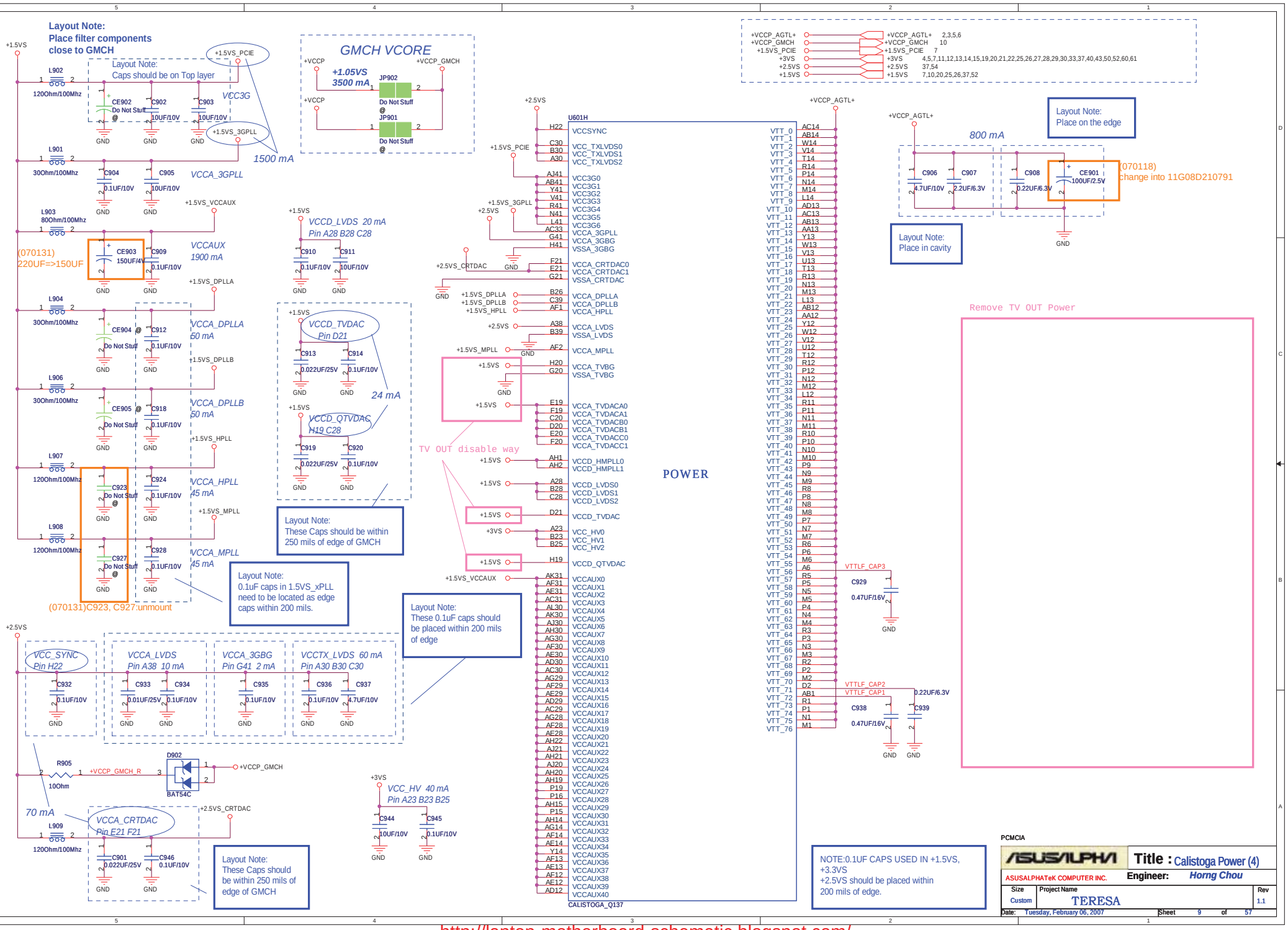
Date: Tuesday, February 06, 2007 Sheet 6 of 57

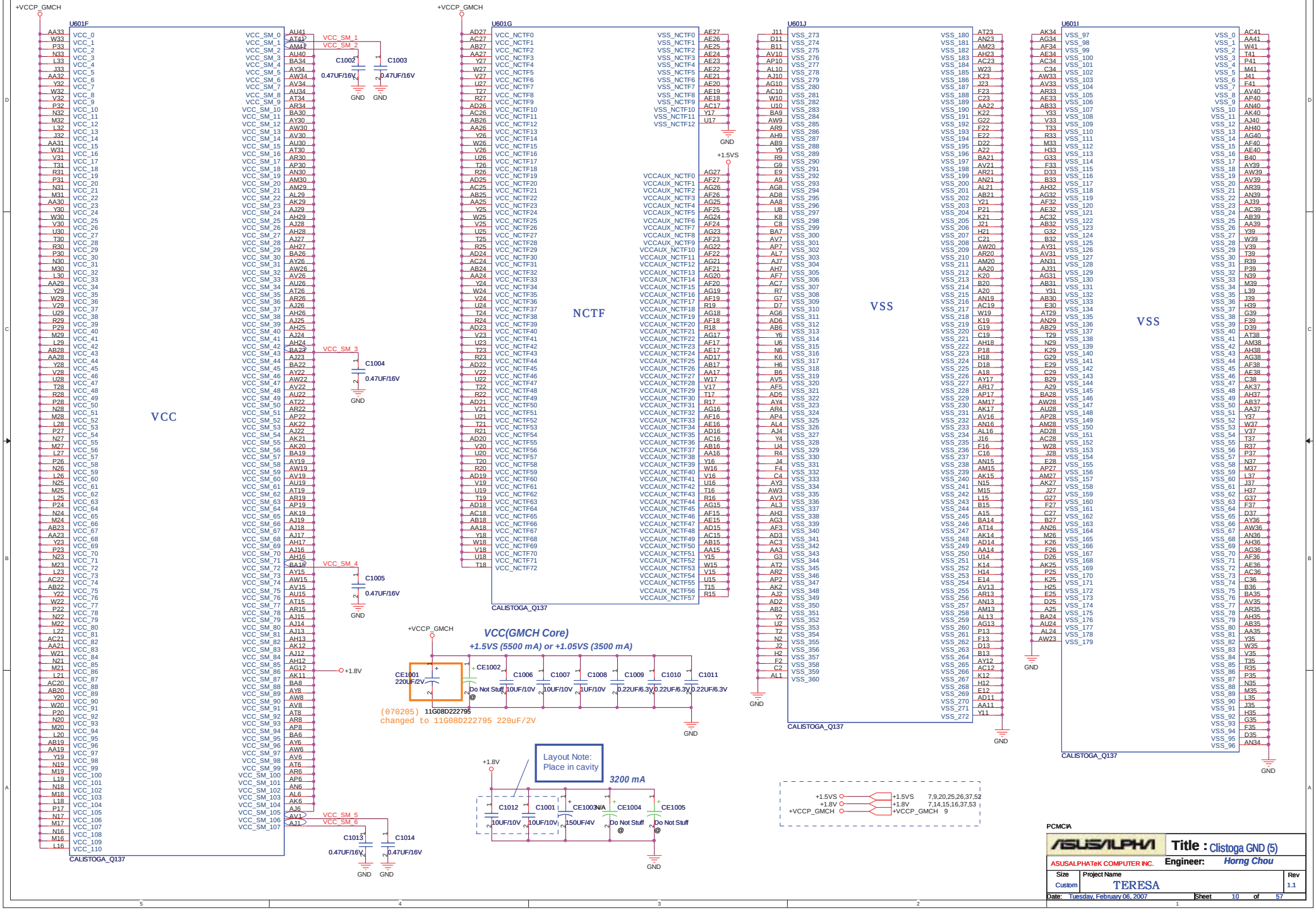


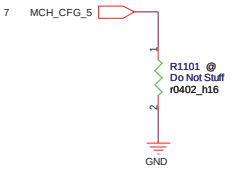


PCMCIA

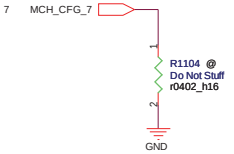
ASUSALPHA	Title : Calistoga DDR2 (3)	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 8 of 57	



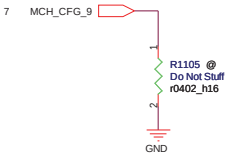




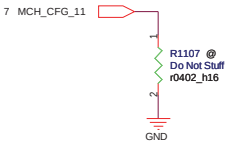
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



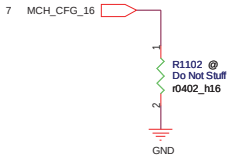
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



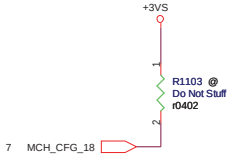
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



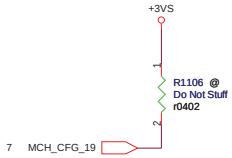
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

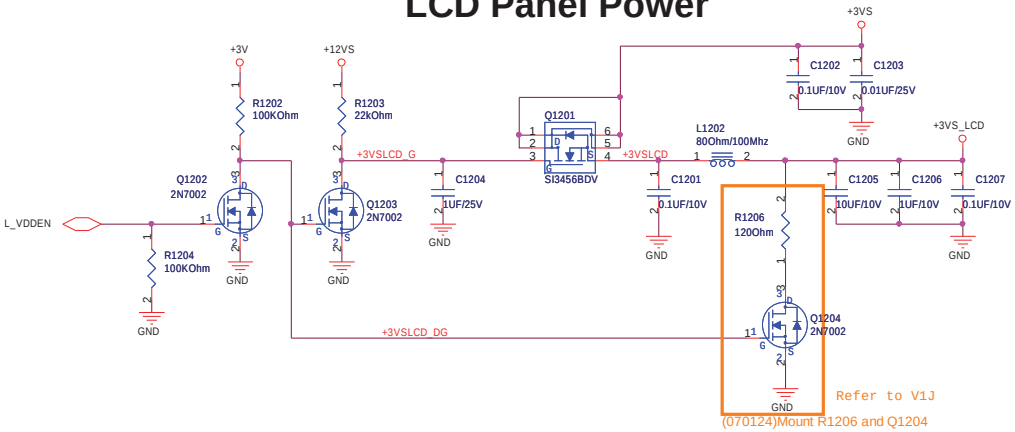
CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

(061215)Remove +2.5VS power supply

PCMCIA
ASUSALPHA
Title : Calistoga Strapping
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size: Custom | Project Name: TERESA | Rev: 1.1
Date: Tuesday, February 06, 2007 | Sheet 11 of 57

LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)



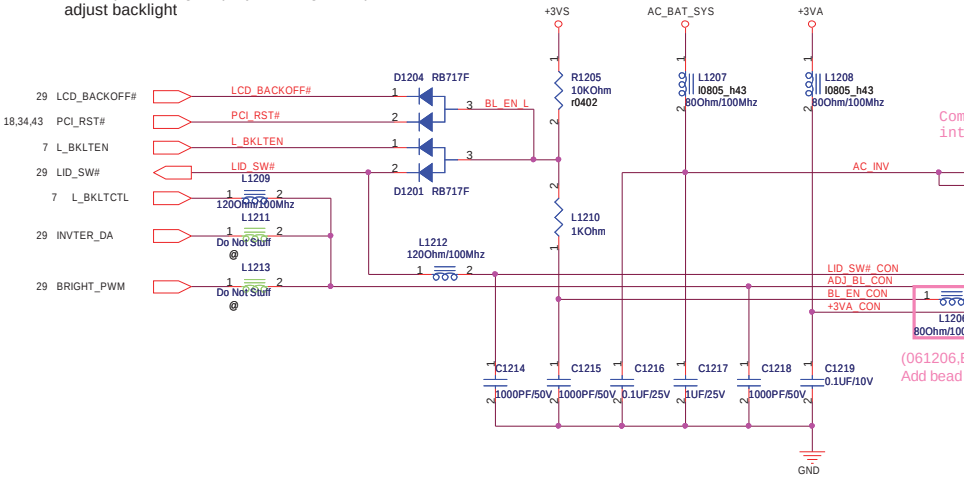
Remove CMOS Camera(USB4)

LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

Inverter Board built in 15.4W LCD Panel



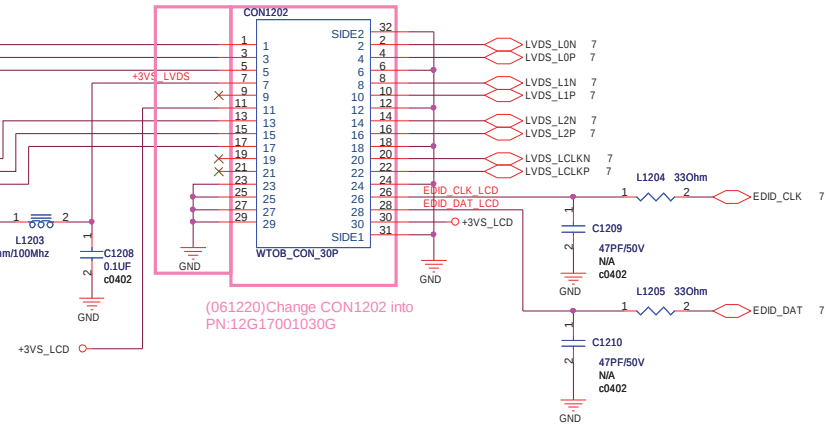
Combine Inverter interface into LVDS interface

(061206,EMI)
Add bead

LCD LVDS & INVERTER Interface

Delete LVDS channel B

Rearrange pin location(061201)



(061220)Change CON1202 into PN:12G17001030G

PCMCIA

ASUSALPHA

Title : LVDS & INVERTER

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

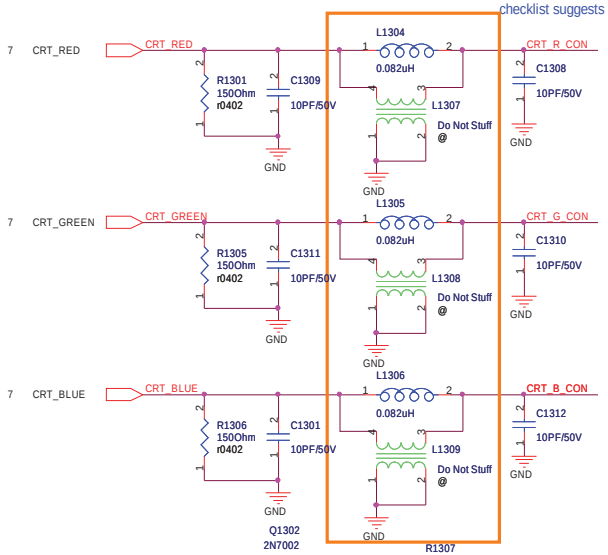
Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 12 of 57

CRT OUT

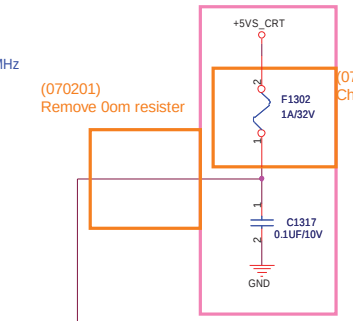
(061206,EMI)
Add L1307, L1308, L1309
(070205) tune performance
changed to 09G023821009 0.082uH

checklist suggests 47ohm/100MHz



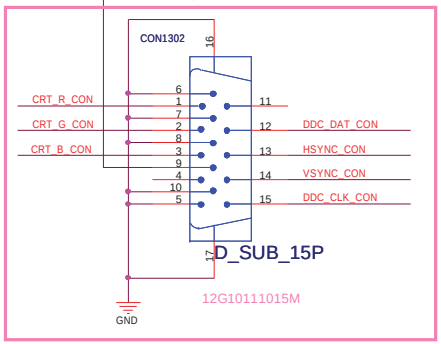
New addition for Teresa

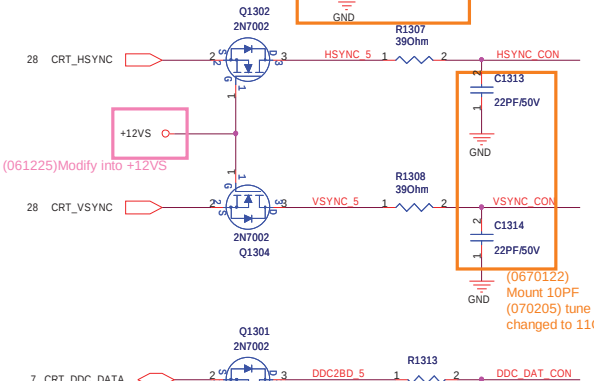
(070201)
Remove 0om resister



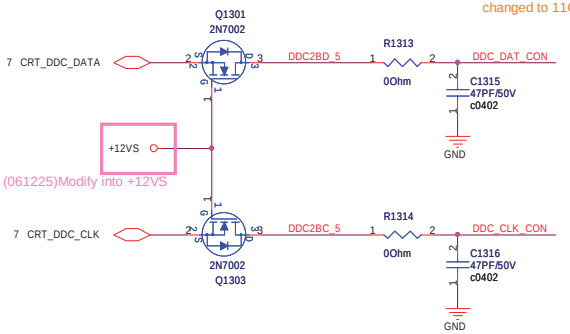
(070130)
Change fuse into 1A

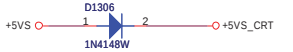
Change D-SUB into PN:12G10111015M

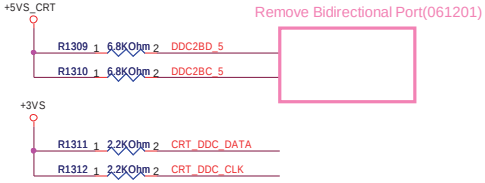




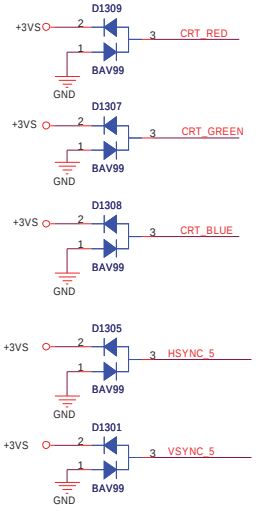
(0670122)
Mount 10PF
(070205) tune performance
changed to 11G232022004360 22pF







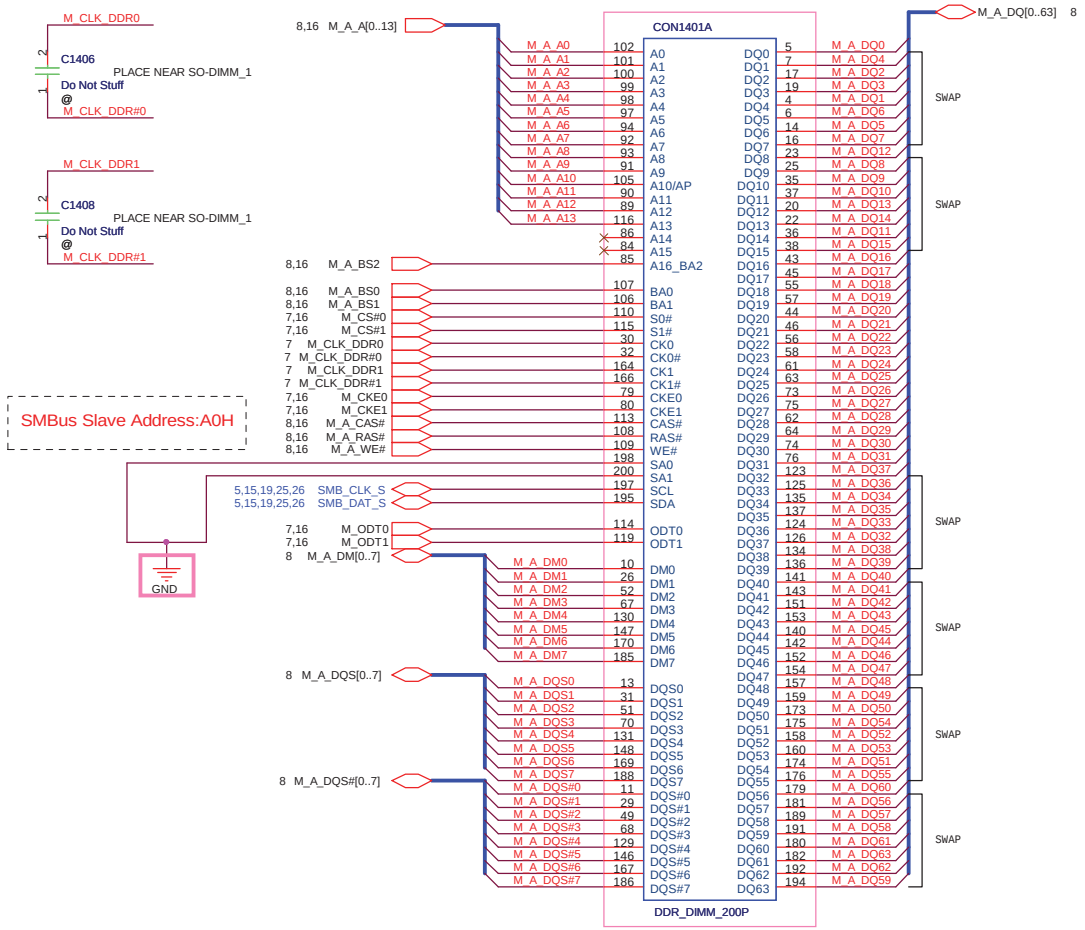
Remove Bidirectional Port(061201)



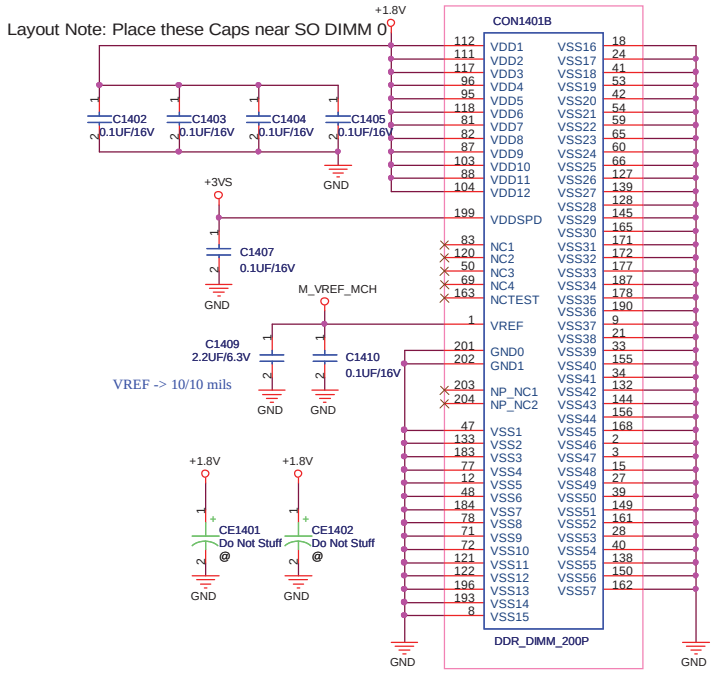
PCMCIA

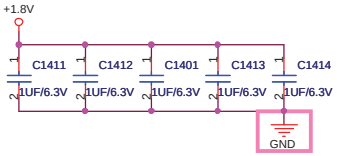
ASUSALPHA	Title : CRT & TV OUT	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 13 of 57	

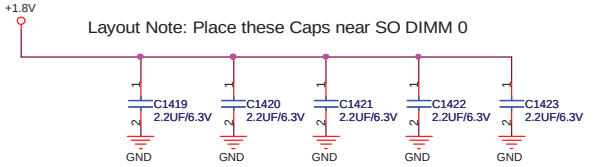
(061221)Change CON1401 into PN:12G02502200R



(061221)Change CON1401 into PN:12G02502200R







SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

PCMCIA

ASUSALPHA	Title : DDR2 SO-DIMM0	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 14 of 57	

SMBus Slave Address:A4H

Address reference +1.8V, add four 0.1uF decoupling CAP.

(061227)Update PCB footprint PN:12G025032008

CON1501A

CON1501B

DDR_DIMM_200P

SWAP

Layout Note: Place these Caps near SO DIMM 0

Layout Note: Place these High-Freq decoupling Caps near the GMCH

Layout Note: Place these CAPs near the GMCH

PLACE NEAR SO-DIMM_0

Do Not Stuff

VREF -> 10/10 mils

10KOhm

+3VS_SET

PCMCIA

ASUSALPHA

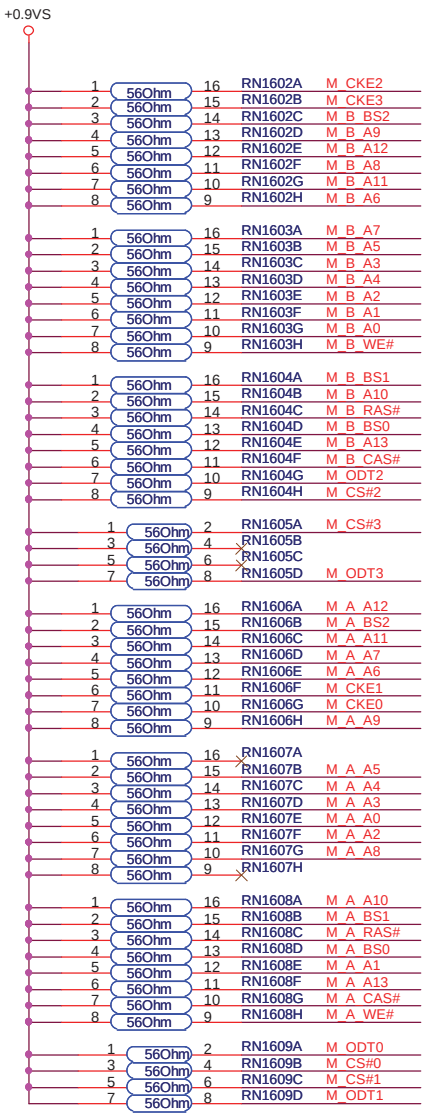
Title : DDR2 SO-DIMM1

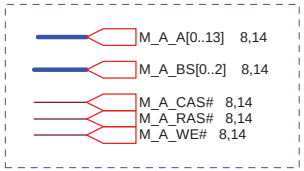
ASUSALPHATeK COMPUTER INC.

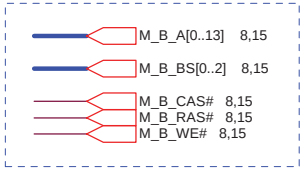
Engineer: Horng Chou

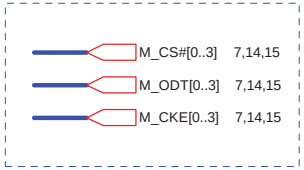
Size	Project Name	Rev
Custom	TERESA	1.1

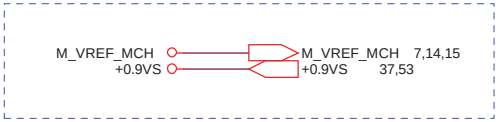
Date: Tuesday, February 06, 2007 Sheet 15 of 57



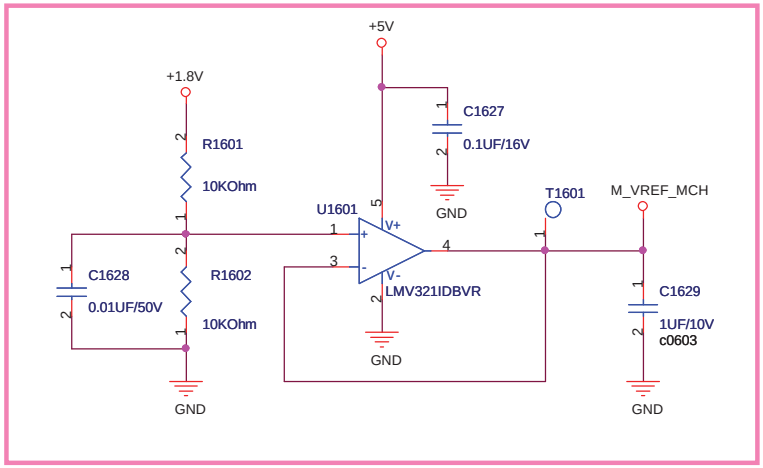


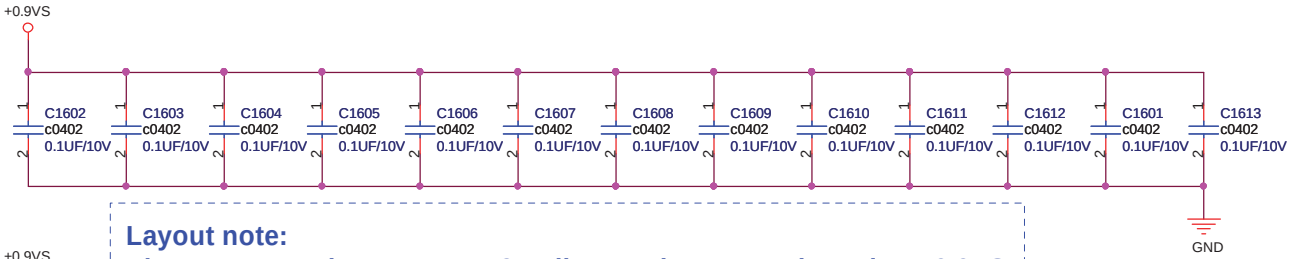




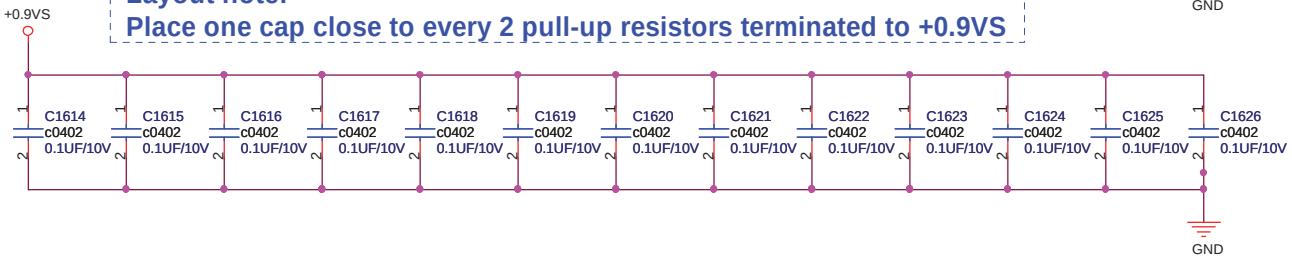


Add Voltage Follower



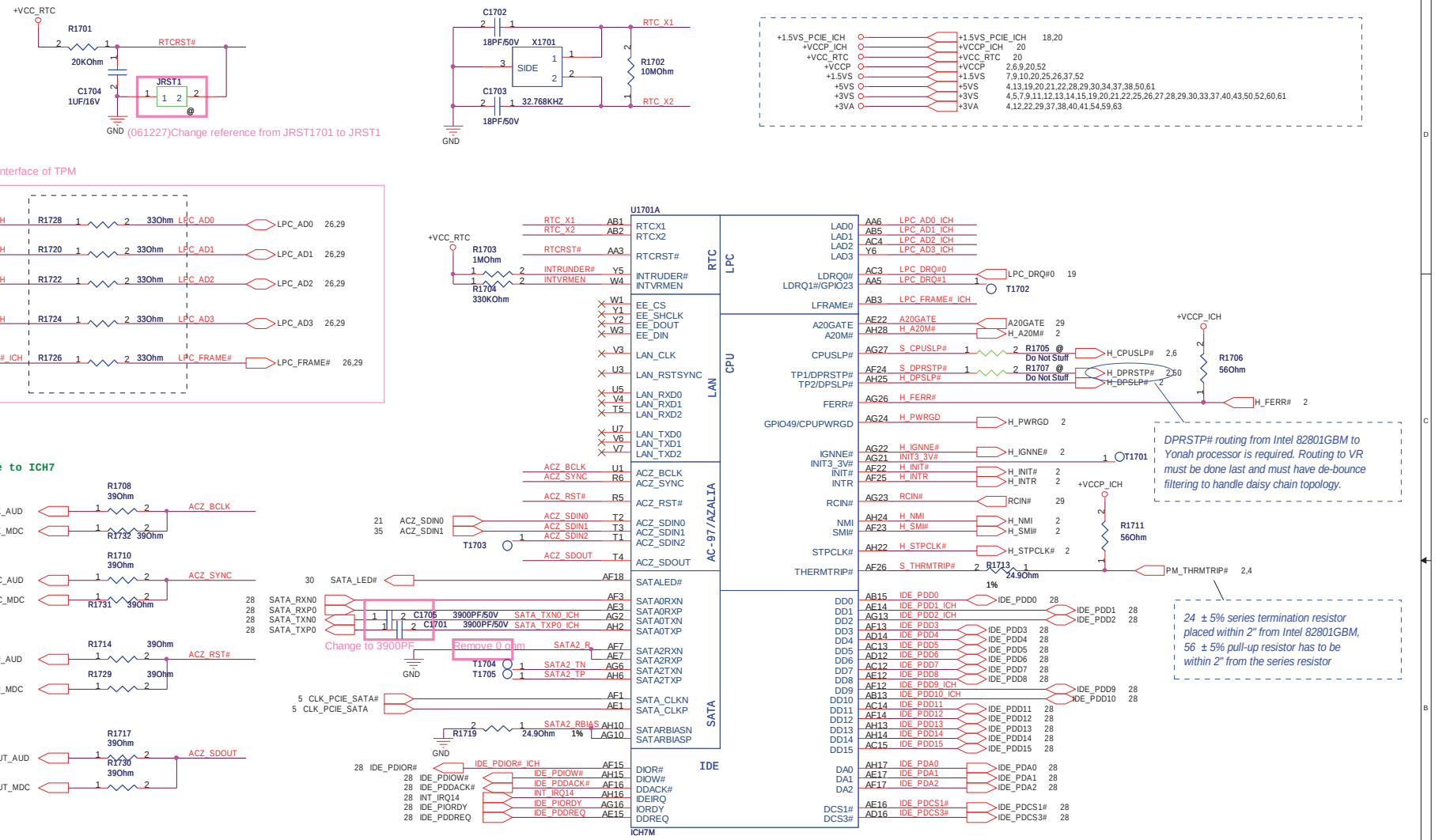


Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS



PCMCIA

ASUSALPHA	Title : DDR2 TERM	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 16 of 57	



PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

(061215)Add AND gates

0ohm replace AND gates

(061204)CRT H/VSYNC buffer circuit move to page-28

Modify USB Device table

USB Devices

Port 0	CON3602
Port 1	Unused
Port 2	CON3601
Port 3	CON3601
Port 4	Unused
Port 5	Unused
Port 6	NewCard
Port 7	Unused

Layout Note:
Pull-ups must be placed within 500 mils from Intel 82801GBM pins

Add test points

PCMCIA

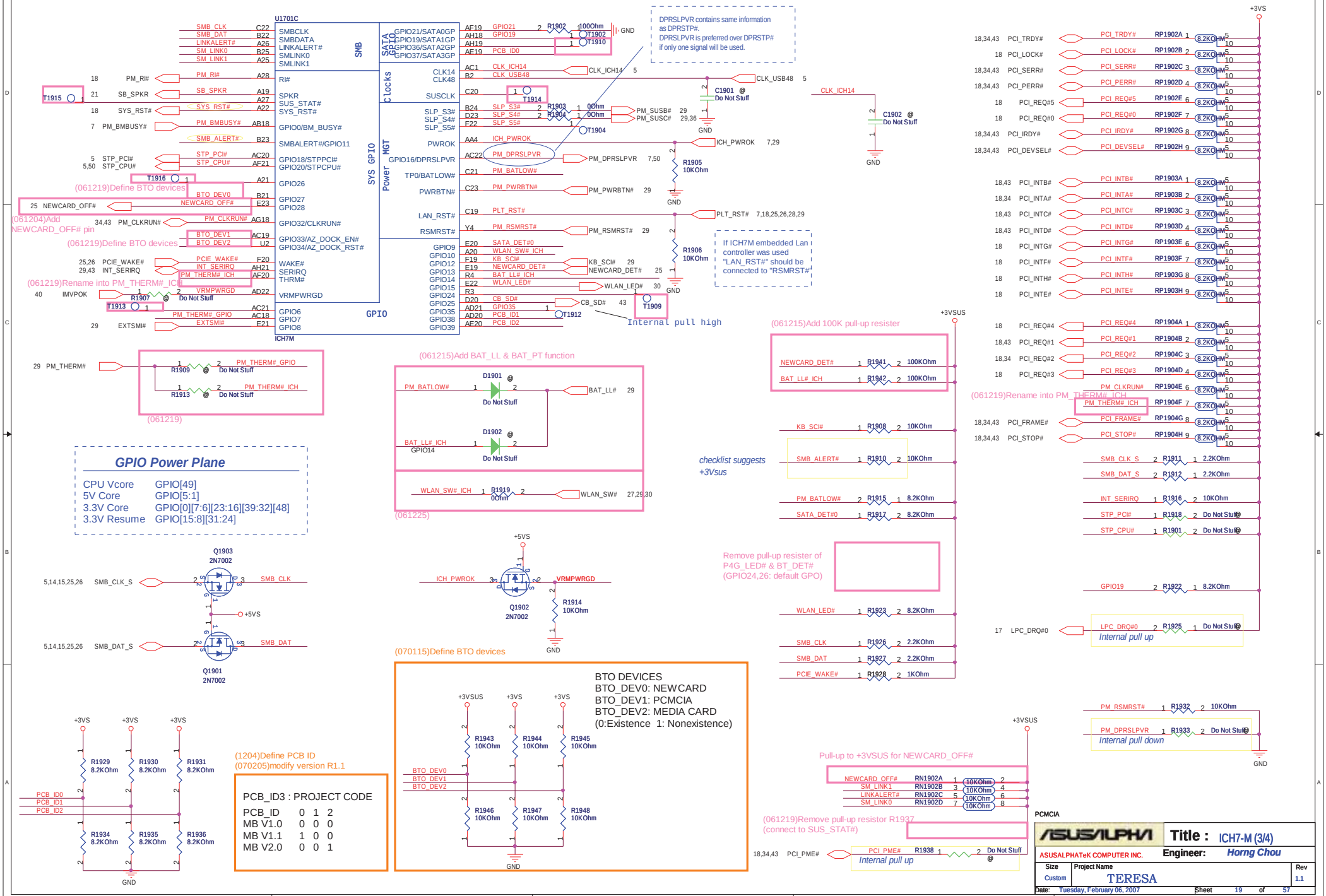
ASUSALPHA

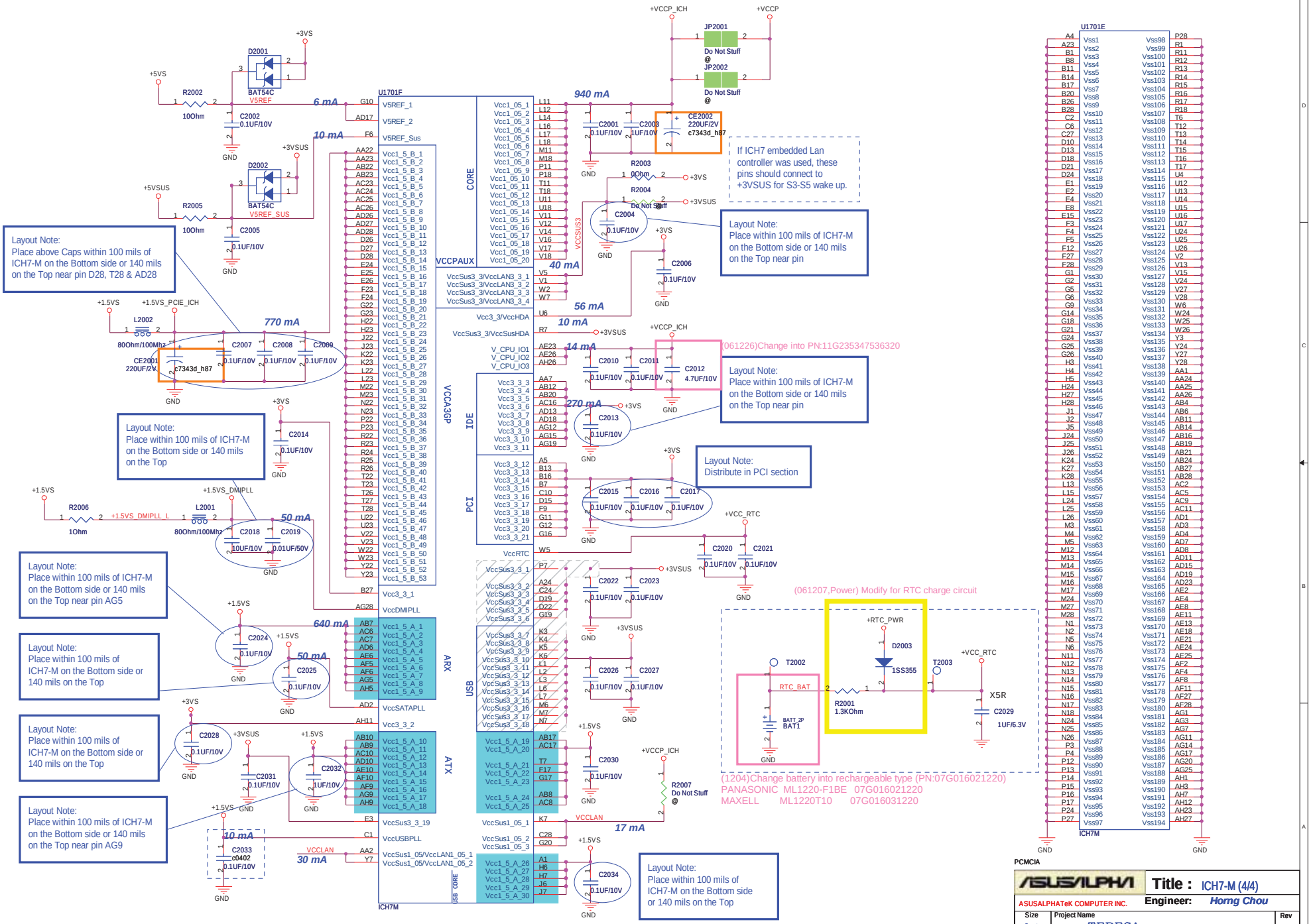
Title : ICH7-M (2/4)

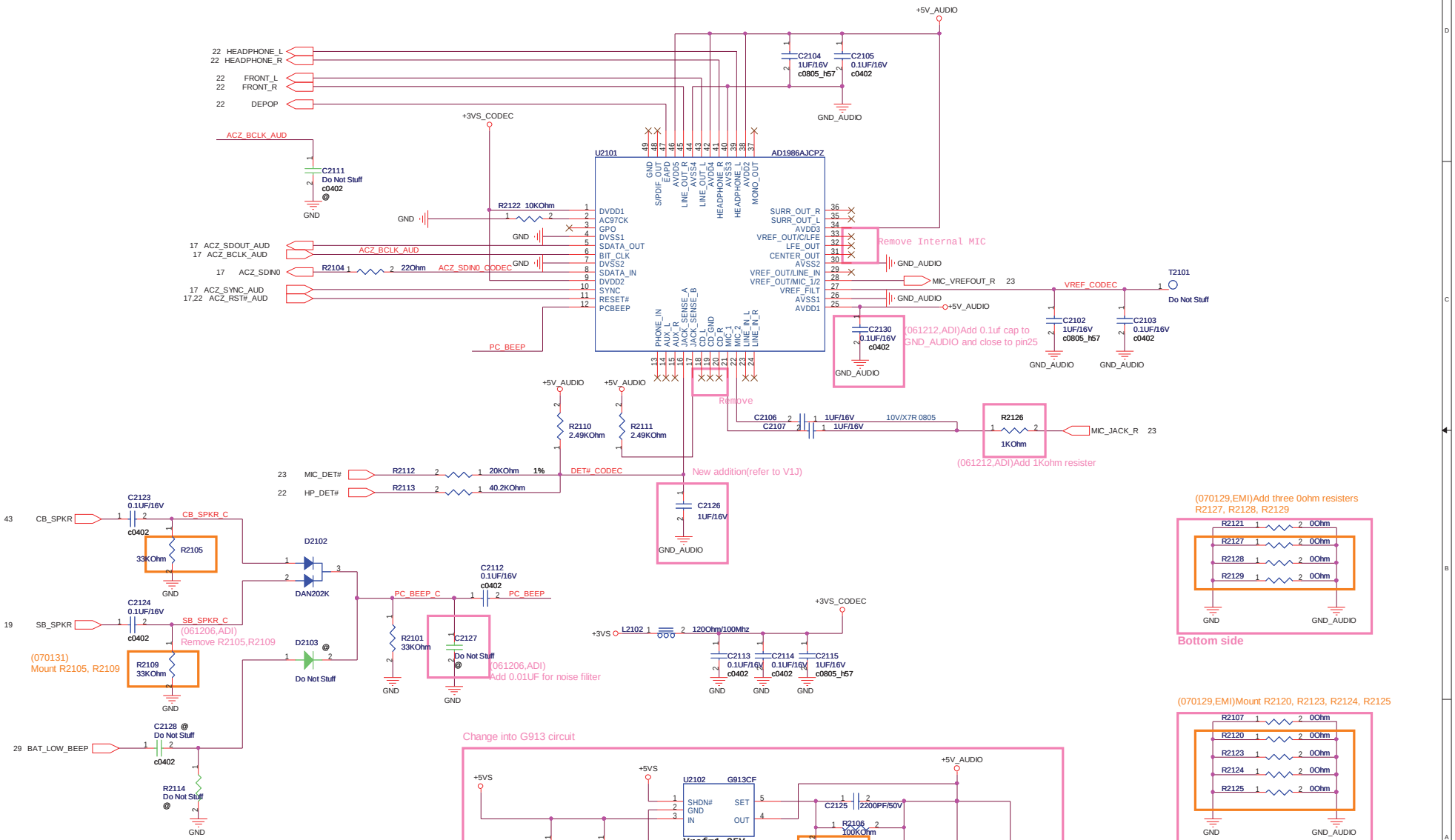
ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

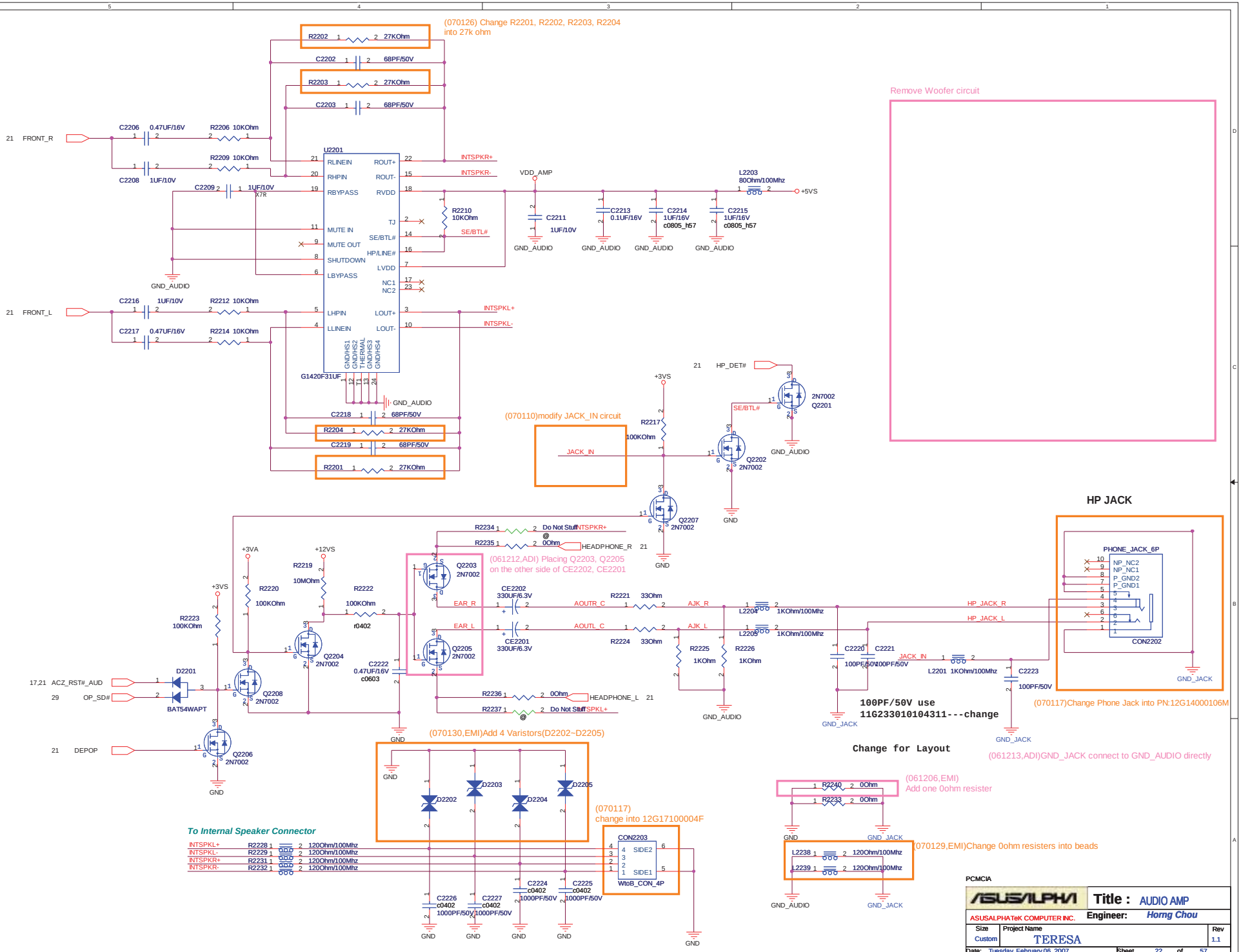
Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 18 of 57





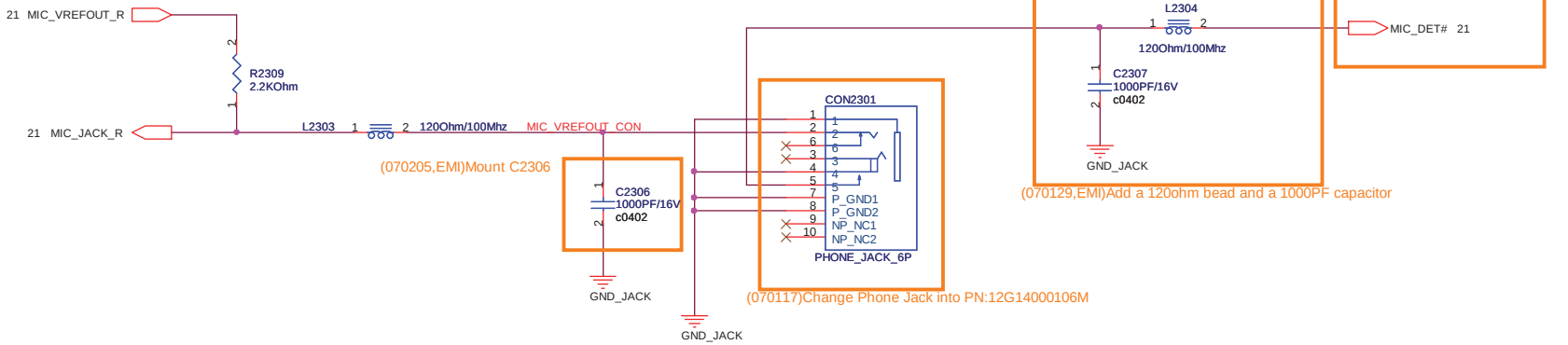




Remove Internal MIC pre-Amplifier

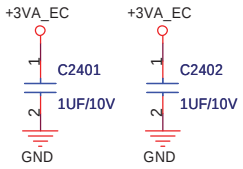
(070110)modify MIC_DET# circuit

MICROPHONE IN

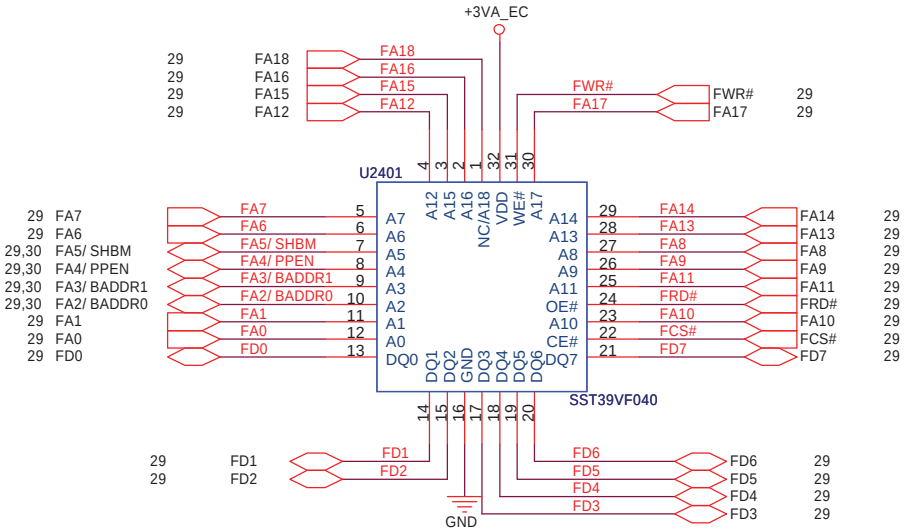


PCMCIA

ASUSALPHA	Title : MIC JACK
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou
Size: Custom	Project Name: TERESA
Rev: 1.1	
Date: Tuesday, February 06, 2007	Sheet 23 of 57



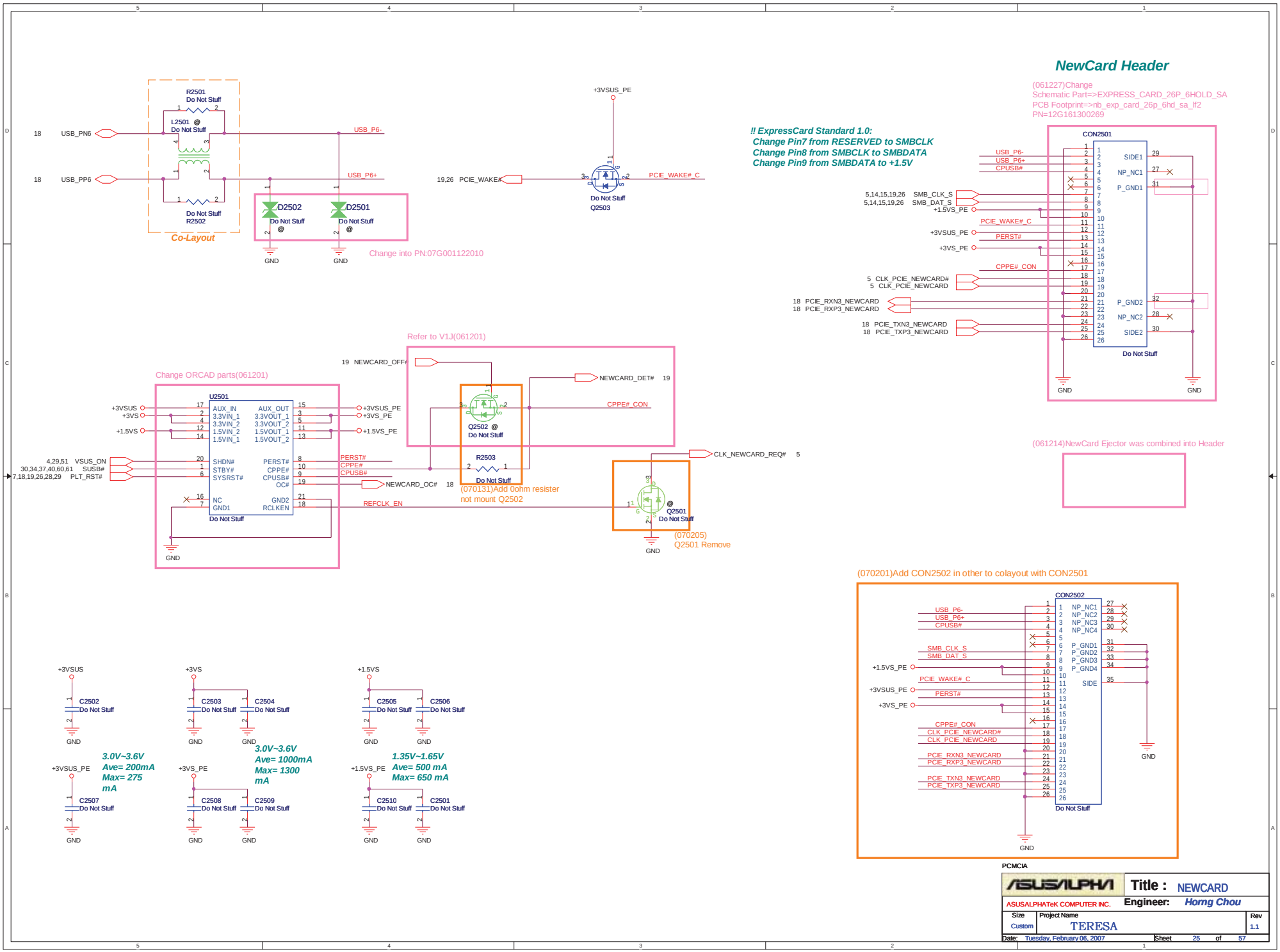
ISA ROM



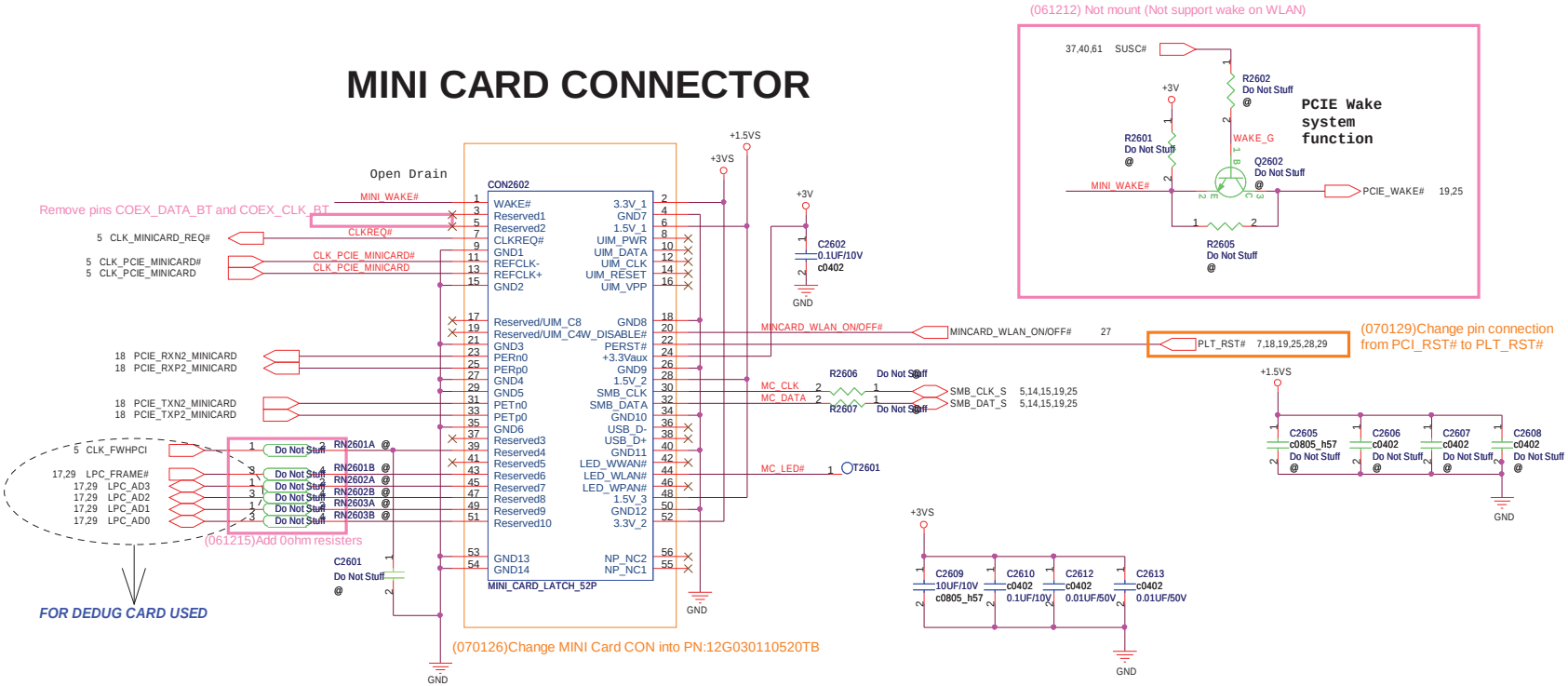
(070205)05G001014110
2nd: 05G001027221

PCMCIA

ASUSALPHA	Title : ISA ROM	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 24 of 57	

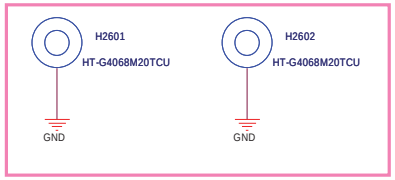


MINI CARD CONNECTOR



Check O/D output or push pull

Instead of Mini-PCIE latch connecter.For cost down.



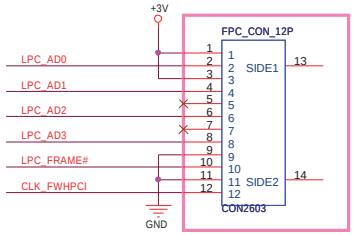
(070201)Change MINI Card NUT into PN:13G021056061TB

WLAN SPEC:

		WLL3140	WLL4080
Transmit Mode Current	11.a		550mA
	11.b	525mA	560mA
	11.g	560mA	550mA
	11.n		
Receive Mode Current	11.a		280mA
	11.b	430mA	270mA
	11.g	460mA	280mA
	11.n		
Sleep Mode Current		220mA	20mA
Supplied Voltage(VCC)	MIN	3.0V	3.0V
	TYP	3.3V	3.3V
	MAX	3.6V	3.6V

Debug Card CON

(061206)Change Debug CON into PN:12G18340120E



PCMCIA

ASUSALPHA | Title : MINI PCIEX/DEBUG CON

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

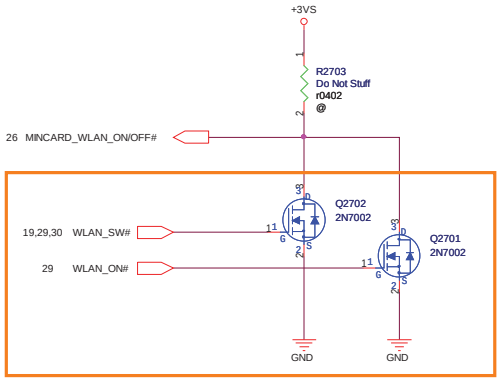
Date: Tuesday, February 06, 2007 Sheet 26 of 57

For Bluetooth

Deltete Bluetooth CON

For Side SW

WLAN ON/OFF Control



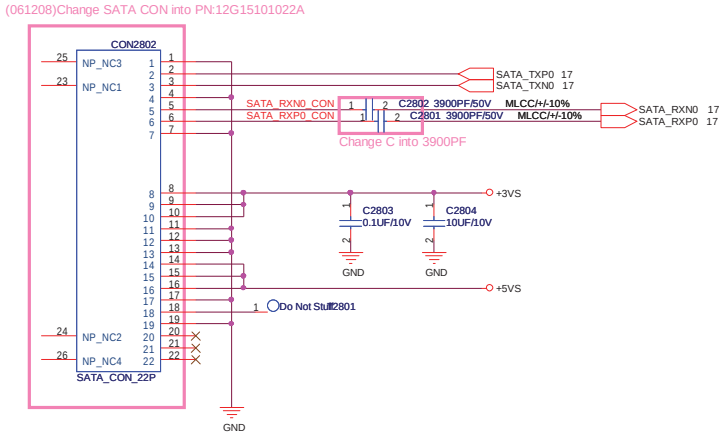
(070202)Modify WLAN on/off circuit

Deltete BT ON/OFF Control

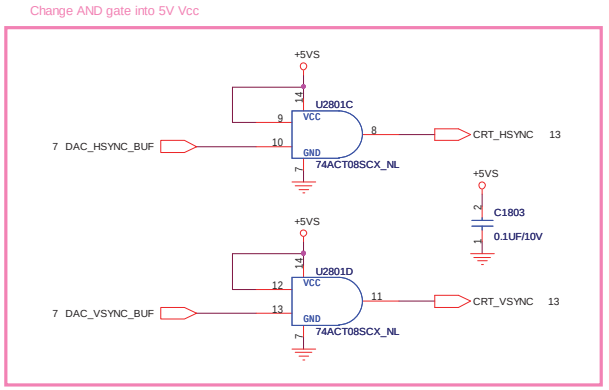
Deltete FR Switch

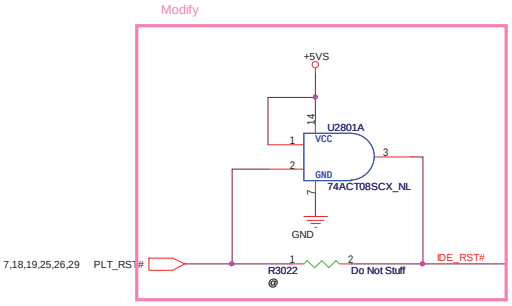
PCMCIA

ASUSALPHA	Title : WLAN CONTROL	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 27 of 57	

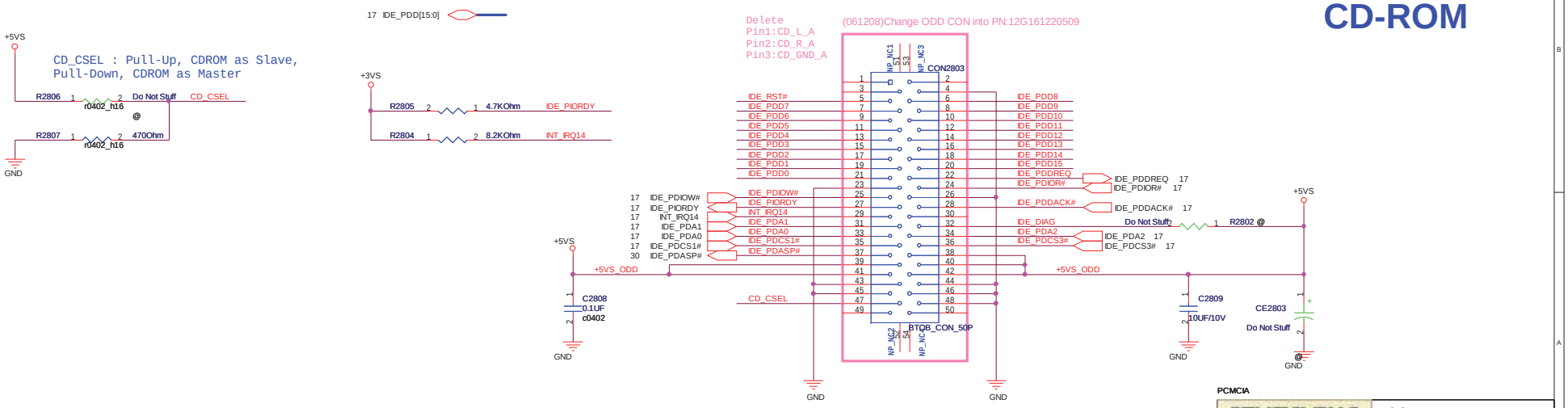


SATA HDD



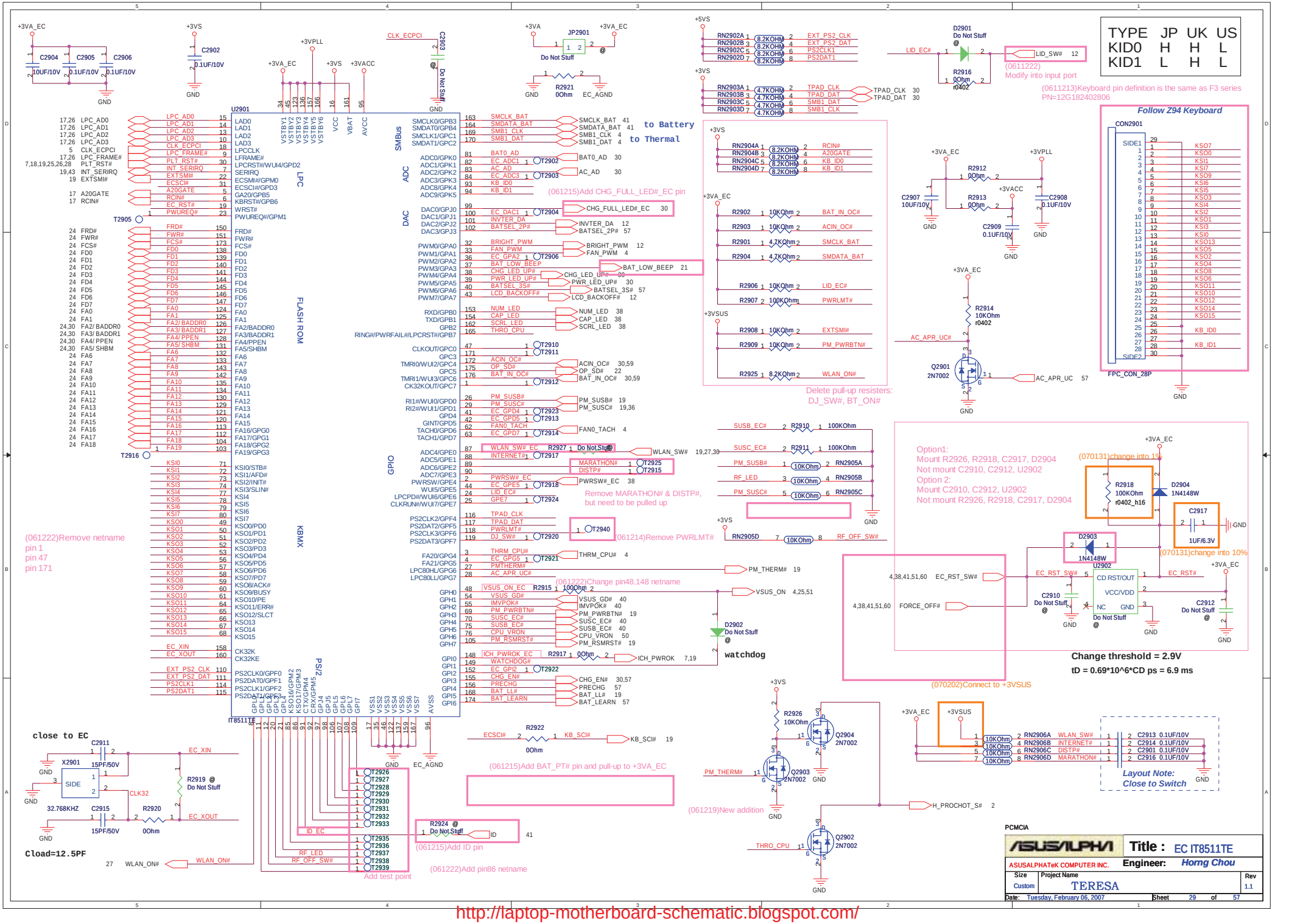


CD-ROM



PCMCIA

ASUSALPHA	Title :	PATA-SATA & ODD
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 28 of 57	



EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR

+3VA_EC
R3002 @ Do Not Stuff r0402
FA2/ BADDR0
FA2/ BADDR0 24,29
R3006 10KOhm r0402
GND

+3VA_EC
R3003 10KOhm r0402
FA3/ BADDR1
FA3/ BADDR1 24,29
R3007 @ Do Not Stuff r0402
GND

BADDR[1:0]

No pull up:	The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:	The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:	The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

EC ADC

Battery

BAT 16.8V
R3004 @ Do Not Stuff r0402_h16
BAT0_R_AD
R3005 @ Do Not Stuff
BAT0_AD 29
R3008 @ Do Not Stuff
D3002 @ Do Not Stuff
D3003 @ Do Not Stuff
C3002 @ Do Not Stuff c0402
+3VACC
GND

Share Memory

+3VA_EC
R3010 10KOhm r0402
FA5/ SHBM
FA5/ SHBM 24,29
R3013 @ Do Not Stuff r0402
GND

SHBM

No pull up:	Disable shared memory with host BIOS
Ext 10K up:	Enable shared memory with host BIOS

+3VA_EC
R3001 @ Do Not Stuff r0402
FA4/ PPEN
FA4/ PPEN 24,29
R3014 10KOhm r0402
GND

PPEN

No pull up:	Normal
Ext 10K up:	KBS interface pins are switched to parallel port interface for in-system programming.

Adaptor

A/D_DOCK_IN 19V
R3009 @ Do Not Stuff
AC_R_AD
R3011 @ Do Not Stuff
AC_AD 29
R3012 @ Do Not Stuff
D3001 @ Do Not Stuff
D3004 @ Do Not Stuff
C3003 @ Do Not Stuff c0402
+3VACC
3V
2.99V
GND
(070205,EMI)Mount

LED Board Interface

(070131,EMI)New addition for EMI
(070205)mount
Connect to LED Board FFC
D3009 0603-050E101NP-LF
(061219)New addition for EMI
+5VSUS
+5V
C3008 0.01UF/25V
C3007 0.1UF/10V
HDD_LED#
802_LED#_R
CHG_LED#_R
PWR_LED#_R
SUSPEND_LED#
L3024 L3025 L3026 L3027 L3028 L3029 L3030 120Ohm/100Mhz
CON3001
SIDE1 SIDE2
FPC_CON_12P
+5VS
L3002 80Ohm/100Mhz
+5VS_TP
GND
19,27,29 WLAN_SW#
WLAN_SW#
CHG_FULL_LED#
L3031 L3032 120Ohm/100Mhz
C3006 0.1UF/10V
Change LED CON into PN:12G18340120E

Touchpad Board Interface

Connect to Touchpad Board FFC
+5VS_TP
29 TPAD_DAT
29 TPAD_CLK
CON3002
SIDE1 SIDE2
FPC_CON_6P
C3009 0.1UF/10V
C3011 100PF/50V
C3012 100PF/50V
GND GND
(061215)Change TP CON into PN:12G18340060D
(070129,EMI)add two 100PF capacitors

HDD LED

+3VS +5VS
R3019 10KOhm
R3020 Do Not Stuff @
17 SATA_LED#
28 IDE_PDASP#
D3005
HDD_LED#
Do Not Stuff @
D3008
1N4148W
(061212)Modify HDD LED circuit

(061201)Modify Charge & Power circuit

CHARGE LED

+5VSUS
R3015 10KOhm
CHG_LED#_R
ORANGE
T3001
Q3003 2N7002
Q3001 2N7002
29 CHG_LED_UP#
GND

Solution 1
+3VSUS
D3007 @ Do Not Stuff
R3021 @ Do Not Stuff
U3001
C3010 Do Not Stuff @
Do Not Stuff @
Q3006 Do Not Stuff @
Q3011 Do Not Stuff @
29,57 CHG_EN#
29,59 ACIN_OC#
29,59 BAT_IN_OC#
CHG_FULL_LED#
GREEN
Q3005 2N7002
GND

Solution 2
R3023 10KOhm
+5VSUS
29 CHG_FULL_LED#_EC
2N7002 Q3007
GND

POWER LED

25,34,37,40,60,61 SUSB#
D3006 1N4148W
+5V
R3017 10KOhm
PWR_LED#_R
GREEN
Q3008 2N7002
Q3002 2N7002
29 PWR_LED_UP#
GND
SUSPEND_LED#
ORANGE
Q3010 2N7002
GND

(061212)Modify charge full circuit : solution1 & solution2

WLAN LED

+5VS
R3016 10KOhm
802_LED#_R
Remove 0ohm
Remove RF_LED pin
19 WLAN_LED#
Q3009 2N7002
Q3004 2N7002
GND

PCMCIA

ASUSALPHA
Title : EC IT8511/LED&TP CON.
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou

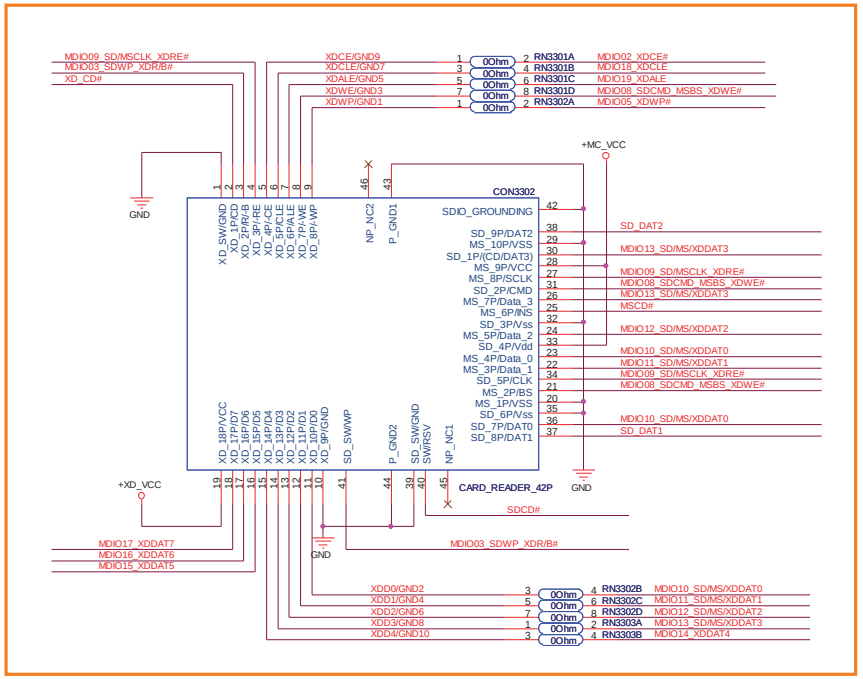
Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 30 of 57

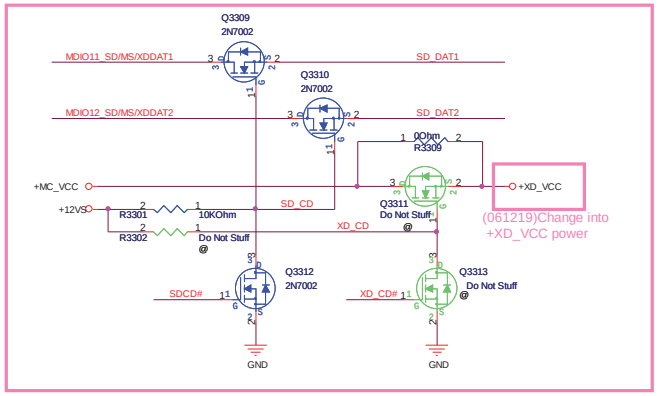
MEDIA CARD SLOT

(070124)Add Media Card CON for colayout

(070130)Add RN3301, RN3302, RN3303



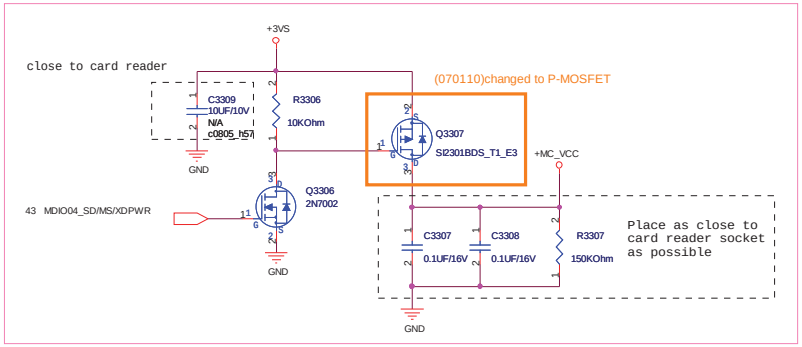
Solve-MS Duo Adaptor short problem / XD short problem



Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

Change circuit from AAT4610A to SI2301

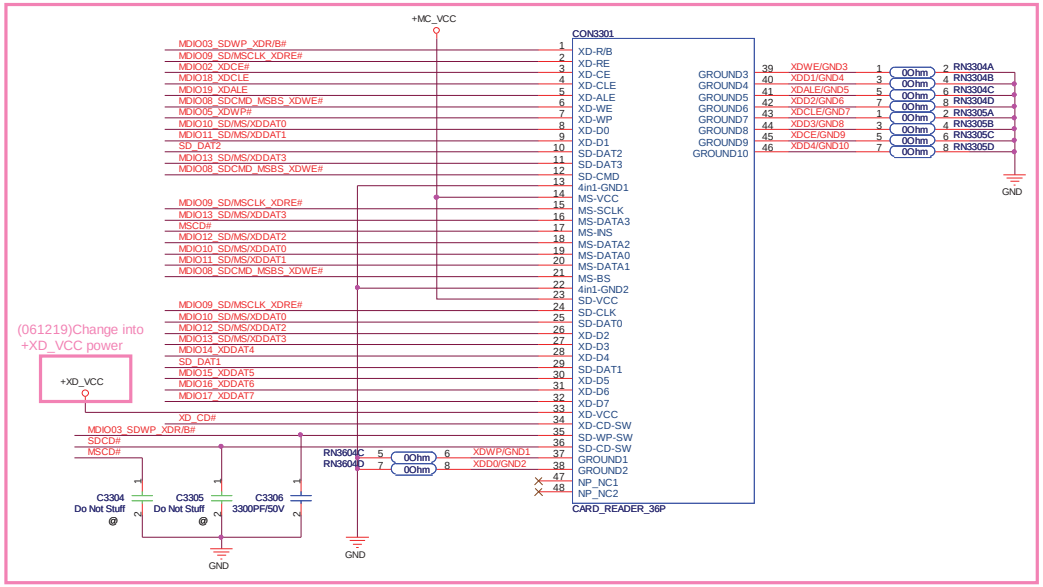


(061208)Change CON3301 into PN:12G340003601

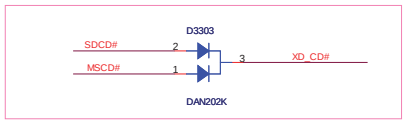
(061225)Change schematic part & PCB Footprint

MEDIA CARD SLOT

(070130)Add RN3303, RN3304, RN3305

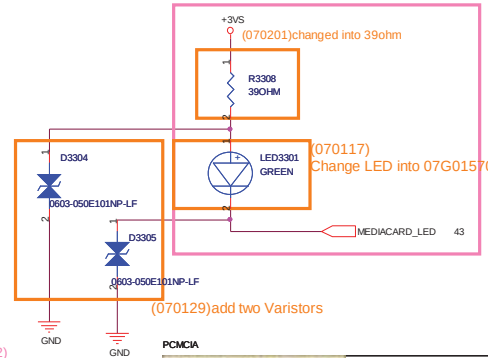


Modify Card Detection Circuit (1/2)



Modify Card Detection Circuit (2/2)

(161219)Change reference into R3308&LED3301



PCMCIA

ASUSALPHAtek COMPUTER INC.

Title : MEDIA CARD SLOT

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 33 of 57

Support Wake On LAN
=>Adapter In mode: S3, S4 and S5
Battery mode: S3

(061207,REALTEK)Connect 0ohm to GND

R3412 Do Not Stuff @

U3401 RTL8100CL

R3408 need close to LAN chip

R3408 5.6KOhm 1%

(061207,REALTEK)Add voltage divider

R3410 1KOhm 1%

R3411 15KOhm 1%

R3409 Do Not Stuff @

R3407 33Ohm

Layout Note:
L_TDP, L_TDN termination resistors
should be near chip

Layout Note:
L_RDP, L_RDN termination resistors
should be near transformer

R3406 3.6KOhm r0402_h16

U3402 AT93C46

(061207)Change to PN:07G010Q12500

X3401 25Mhz

C3406 30PF/50V

C3407 30PF/50V

(070131)change into 30PF

Change trace wide into 30mil

Q3401 MW772M3L 07G003231011

30 mil

(061207,REALTEK)Recommend change to 22UF

L3401 120Ohm/100Mhz

20 mil

30 mil

30 mil

(061207,REALTEK)Remove capacitors

PCMCIA

ASUSALPHATeK COMPUTER INC.

Title : LAN_RTL8100CL

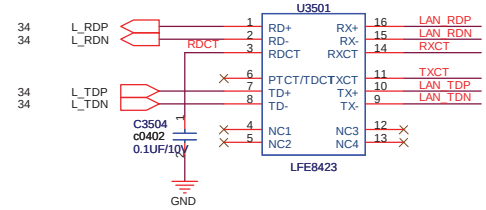
Engineer: Horng Chou

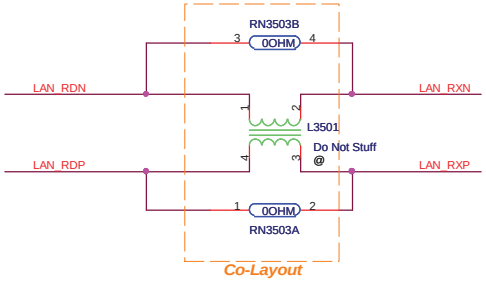
Size	Project Name	Rev
Custom	TERESA	1.1

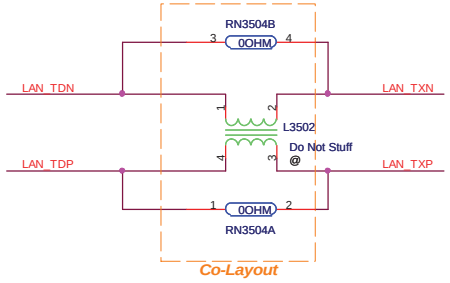
Date: Tuesday, February 06, 2007 Sheet 34 of 57

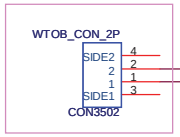
LAN PORT

TRANSFORMER 10/100MB



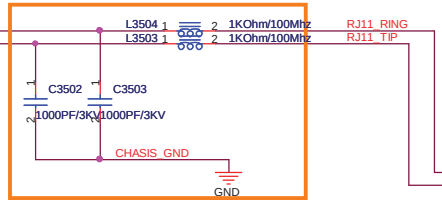




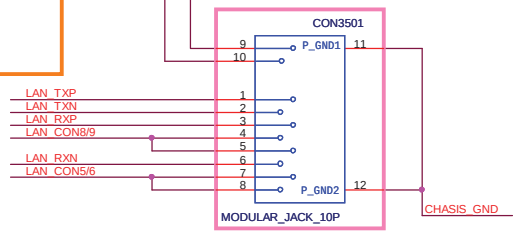


(061214)Change CON3502 into PN:12G17000002B

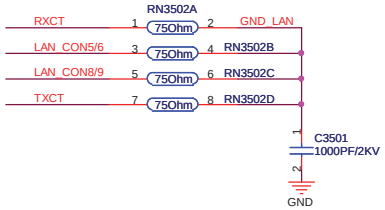
(070131)place C3502, C3503 on the other side of L3503, L3504



RJ11&RJ45



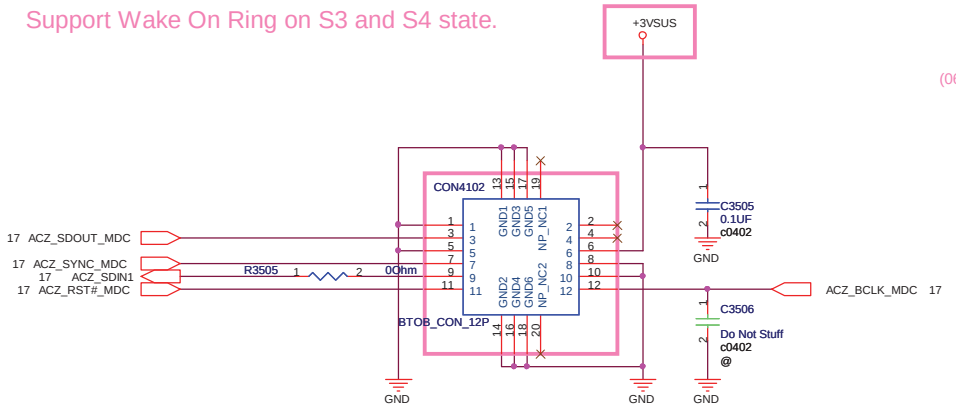
(061214)Change RJ11&RJ45 into PN:12G142011109



MDC CONNECTOR

Support Wake On Ring on S3 and S4 state.

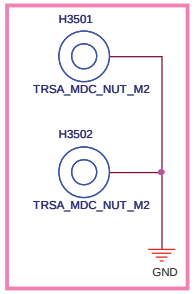
Change power from +3V to +3VSUS



(061214)Change MDC CON into PN:12G16020012D

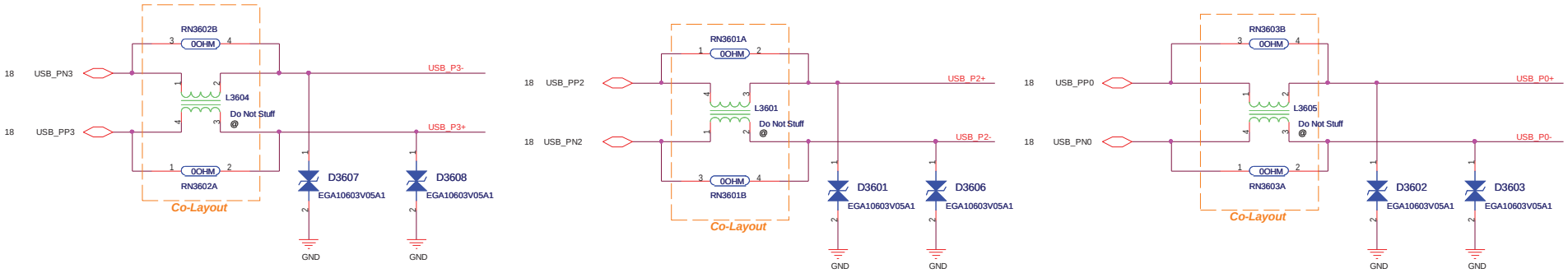
B:MDC NUT

(061219)Change MDC NUT into PN:13G021054000



PCMCIA

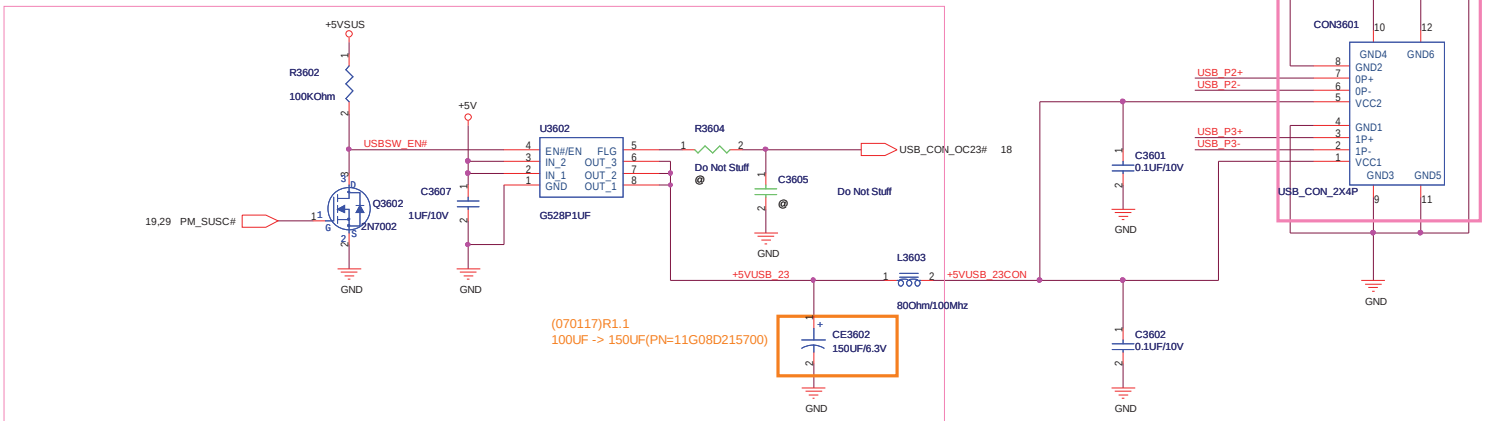
ASUSALPHA	Title : RJ45/RJ11/MDC	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 35 of 57	



Delete N-MOSFET PMN45EN

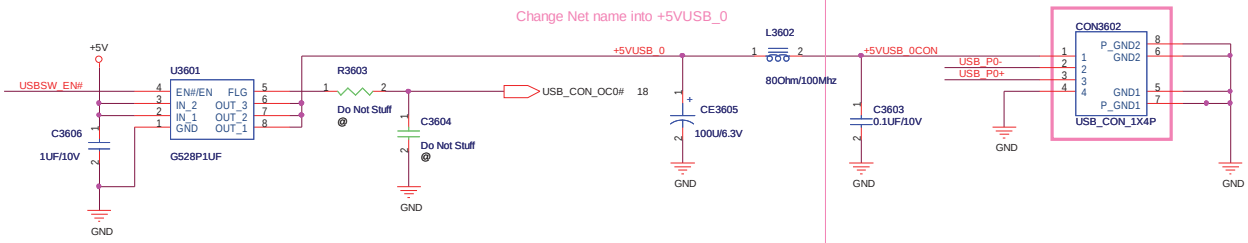
(061211)Change USB CON into PN:12G13111108F

Add USB Switch



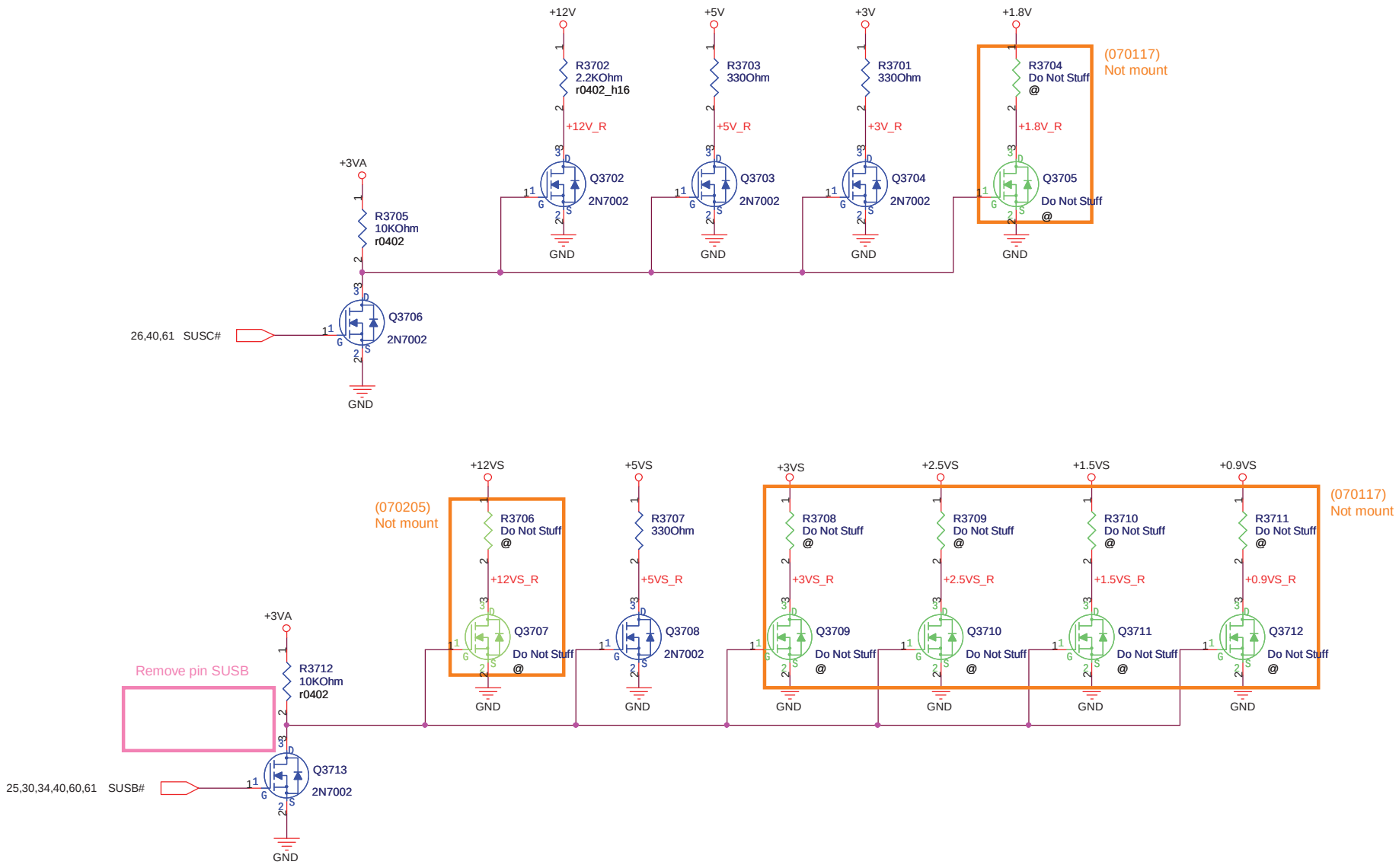
Change Net name into +5VUSB_0

(061206)Change USB CON into PN:12G131030043



PCMCIA

ASUSALPHA	Title : USB CONN x3	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 36 of 57	



PCMCIA

ASUSALPHA

Title : Discharge Circuit

ASUSALPHATeK COMPUTER INC.

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 37 of 57

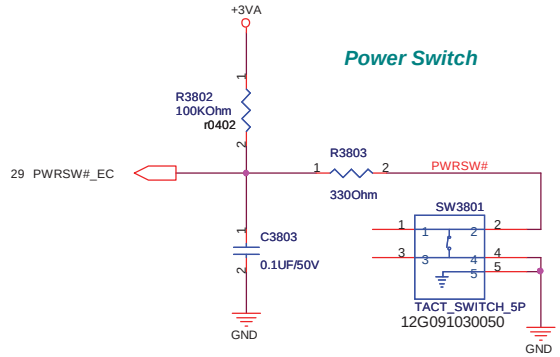
Main Board SW & LED

Power LED move to daughter board

Delete RF/Touchpad and Power4 Gear SWITCH

Delete RF LED and Power4 Gear LED

Power Switch

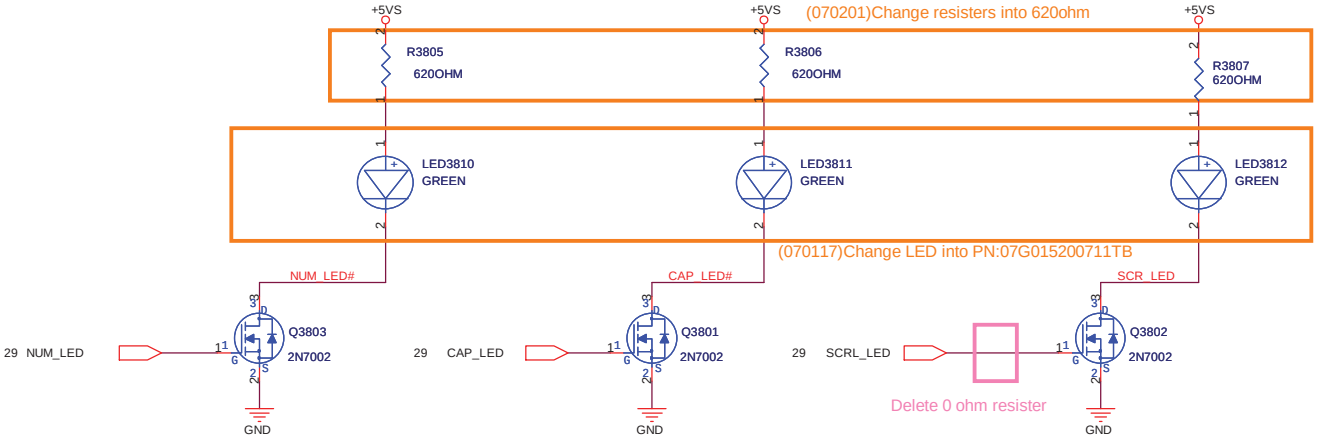


NUMBER LOCK LED

CAPS LOCK LED

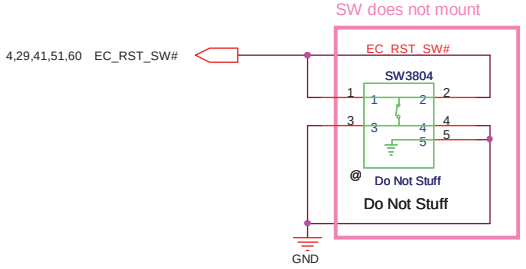
SCROLL LOCK LED

(070201)Change resisters into 620ohm



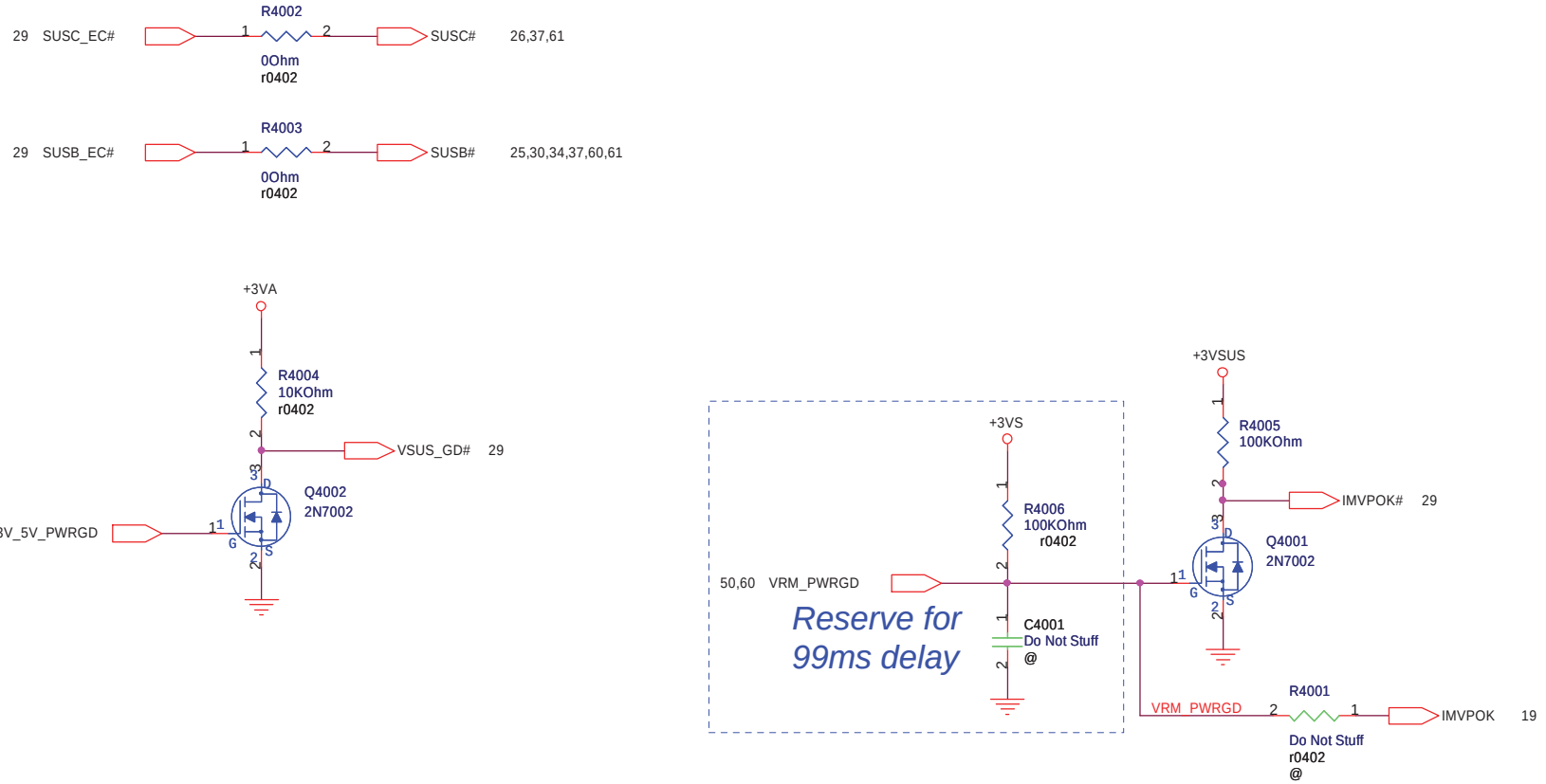
Reset Switch

SW does not mount



PCMCIA

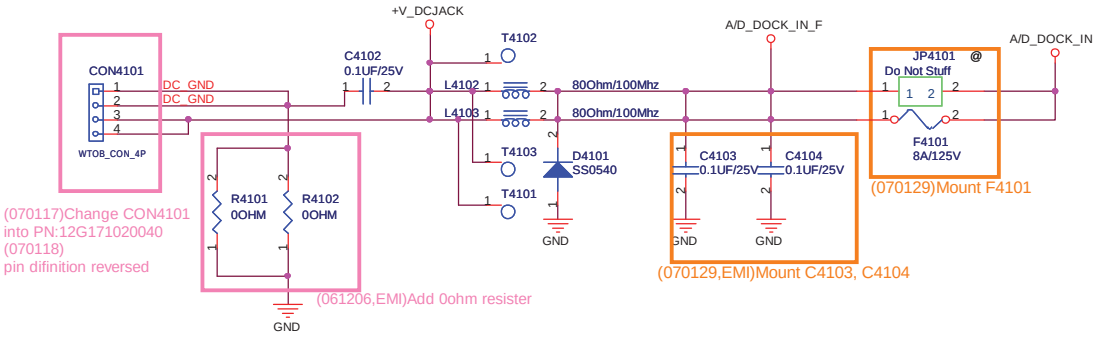
ASUSALPHA	Title : SW/LED	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 38 of 57	



PCMCIA

ASUSALPHA	Title : POWER-ON SEQ.	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 40 of 57	

DC Power Jack



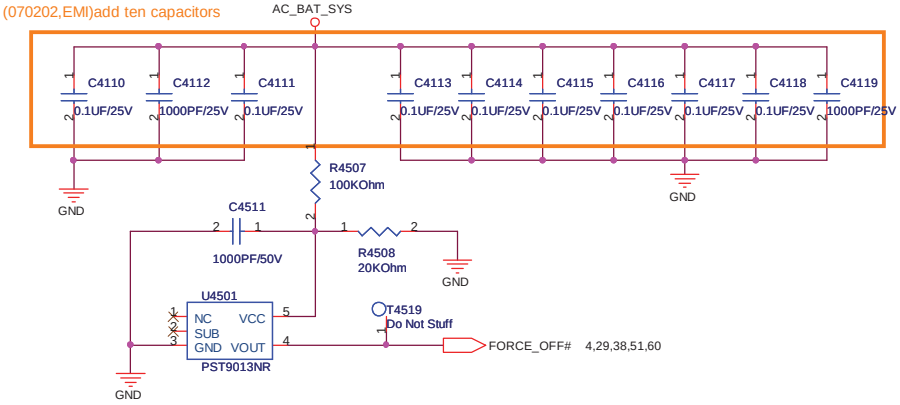
(070117)Change CON4101 into PN:12G171020040 (070118) pin difinition reversed

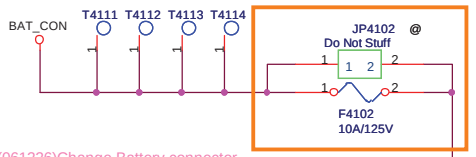
(061206,EMI)Add 0ohm resister

(070129)Mount F4101

(070129,EMI)Mount C4103, C4104

Without Battery & Pull out Adapter

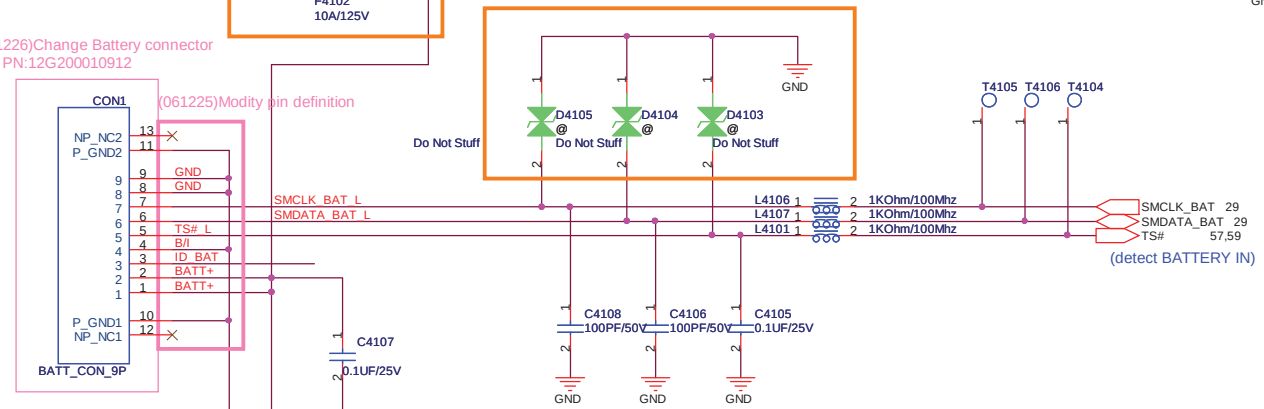




(070130)Add JP4102 and F4102
F4102 must change into 10A(PN=07G012101100I)
(070205)changed to 07G012101100TB

(061226)Change Battery connector into PN:12G200010912

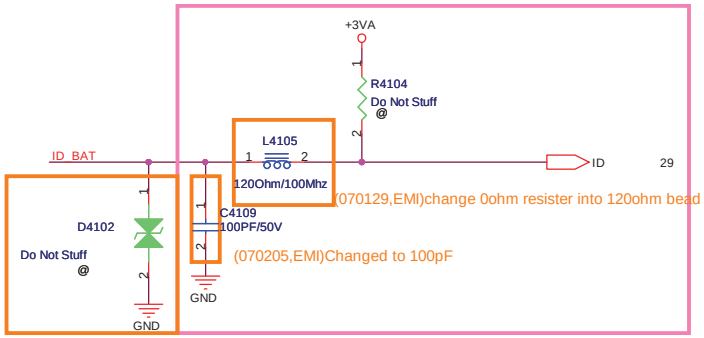
(070129,EMI)add three Varistors



(061225)Modity pin definition

(detect BATTERY IN)

(061219)Connect to EC and pull-up to +3VA



(070129,EMI)change 0ohm resister into 120ohm bead

(070205,EMI)Changed to 100pF

(070129,EMI)add Varistor

(061225)Add R4105 and C4109

PCMCIA

ASUSALPHA

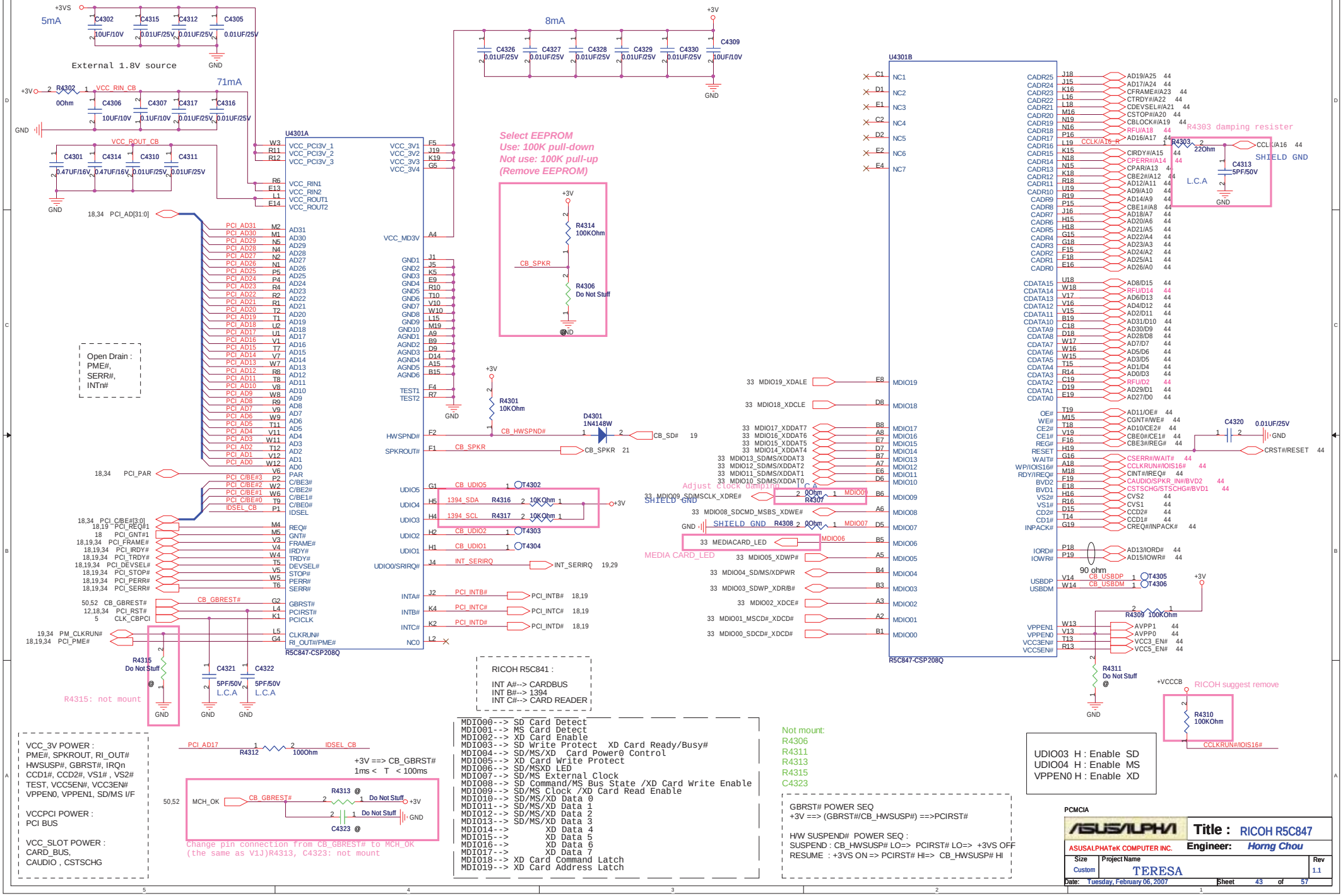
Title : DC/ BATT IN

ASUSALPHATeK COMPUTER INC.

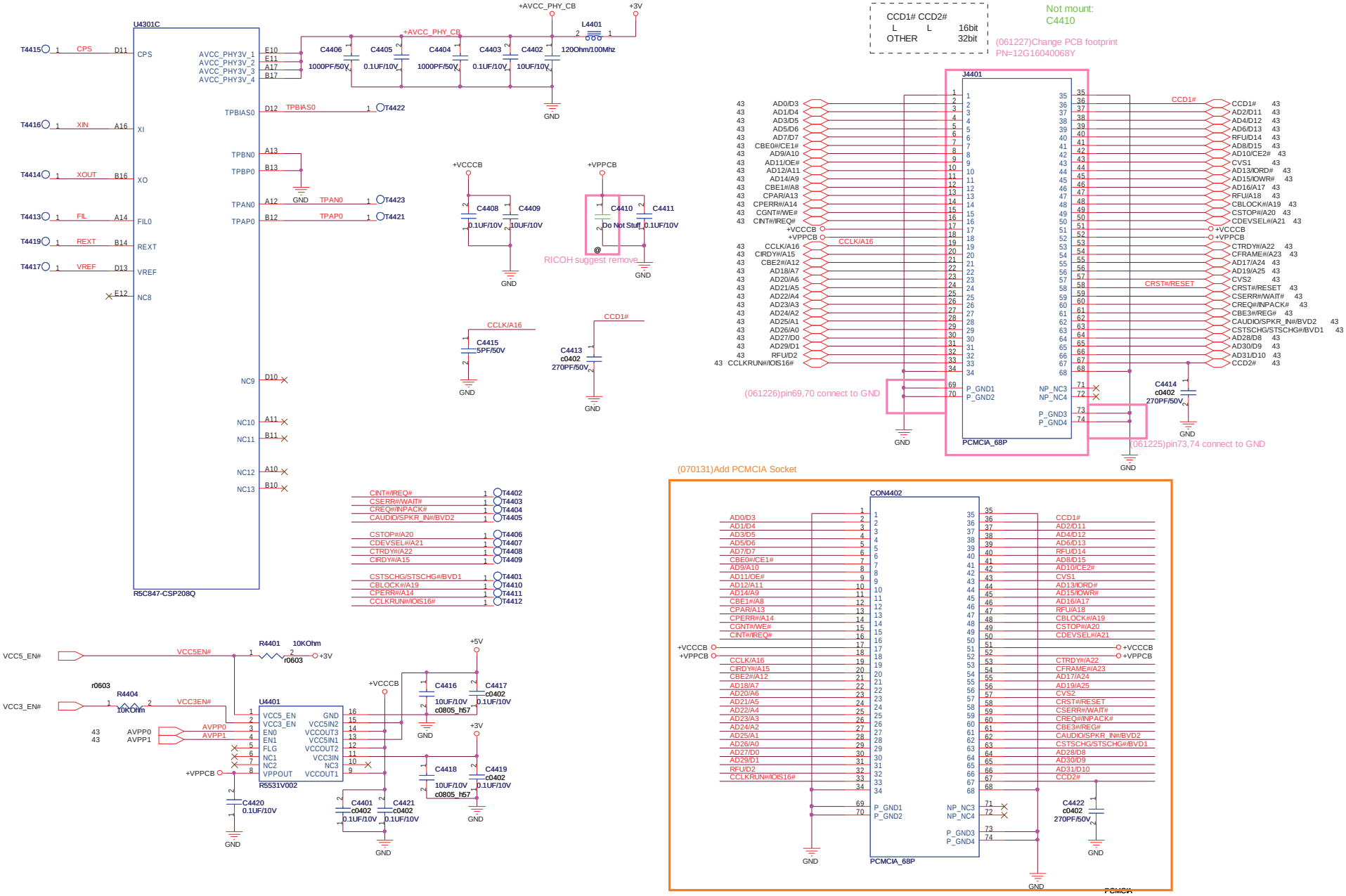
Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 41 of 57



PCMCIA SOCKET



CCD1# CCD2#
L L 16bit
OTHER 32bit

Not mount:
C4410

(061227)Change PCB footprint
PN=12G16040068Y

(061226)pin69,70 connect to GND

(061225)pin73,74 connect to GND

(070131)Add PCMCIA Socket

PCMCIA

ASUSALPHA

Title : CARDBUS SOCKET

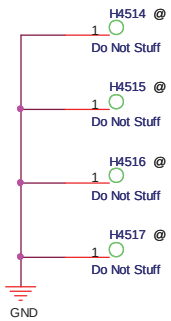
ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 44 of 57

A:CPU BKT

PN:s01756



B:MDC NUT

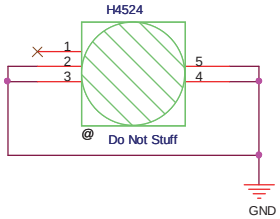
MDC NUT put on page35
(H3501, H3502)

F:MINI CARD NUT

MINI CARD NUT put on
page26(H2601, H2602)

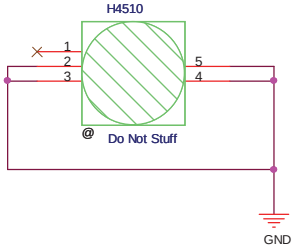
C:TOP TO BTM

PN:S01912



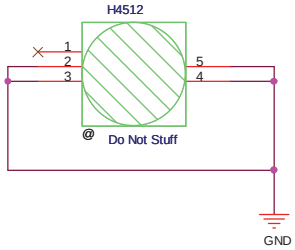
D:FIX MB

PN:s01769



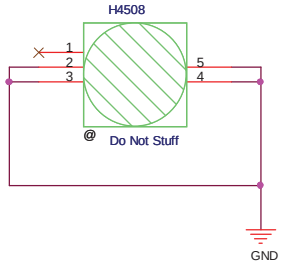
E:TOP TO BTM

PN:S01911



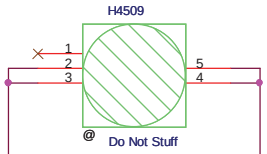
G:FIX MB

PN:s01783



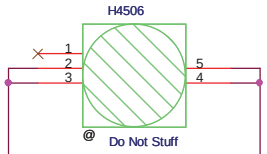
H:SYS BOSS

PN:S01914



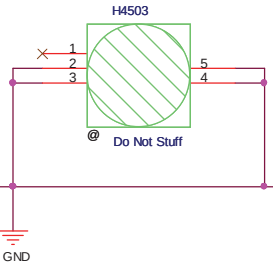
I:MB TO IO BKT

PN:S01913



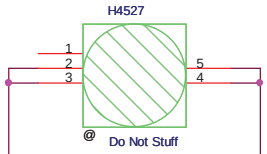
J:SYS BOSS

PN:S01915



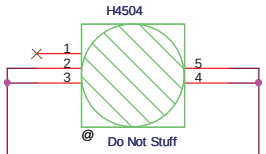
K:MB TO IO BKT

PN:S01705



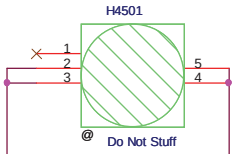
L:TOP TO BTM

PN:S01916



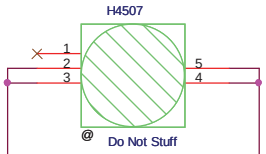
M:SYS BOSS

PN:s01917



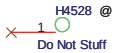
N:TOP TO BTM

PN:S01851



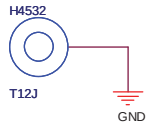
O:ALIGNMENT HOLE

PN:temp_5262_gh15



T:NB SINK NUT

PN:13GNJ510M170-1

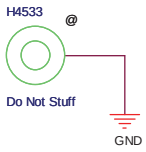


P:ALIGNMENT HOLE

PN:s01724

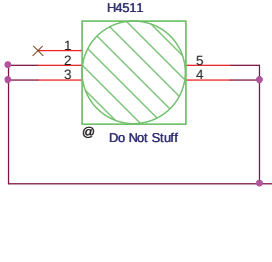
EMI NUT

for LVDS cable
PN:13G021029050



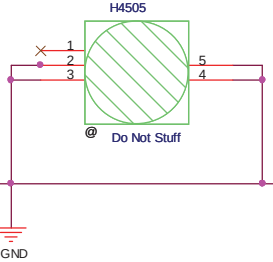
U:TOP TO BTM

PN:S01854



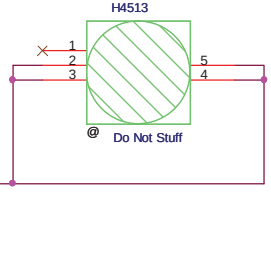
V:TOP TO BTM

PN:S01857



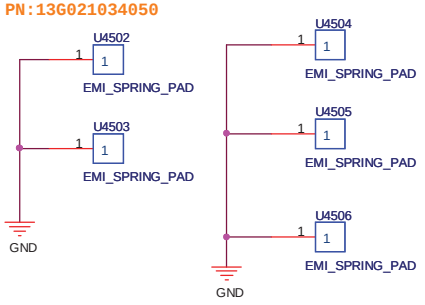
W:TOP TO BTM

PN:S01918



EMI SPRING

PN:13G021034050



PCMCIA

ASUSALPHA	Title : SCREW HOLE	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 45 of 57	

R1.0 to R1.1

Page	Action
3	Change C304, C305, C306, C307, C308, C310, C312, C313 into 10UF for cost down.
4	Add R418 and Q404 to avoid error action.
7	Add R715 and R716 in other to improve signal quality.
12	Mount R1206 and Q1204 in other to reduce discharge time.
13	Change C1313, C1314 into 22PF in other to improve undershoot.
13	Change the rated current of the fuse(F1302) into 1A for customer's demand.
21	Mount R2105 and R2109, or there is no dialing tone.
21	Modify R2108 into 31.6Kohm in other to tune +5V_AUDIO.
21	Add three 0ohm resisters R2127, R2128, R2129 for EMI.
22	Change R2201~R2204 into 27Kohm for speaker volume.
22	Change 0ohm resisters(R2238, R2239) into beads.
22	Remove a N-MOS and a resistor on JACK_IN side due to change a new HP JACK.
22	Add 4 Varistors(D2202~D2205) for EMI.
23	Remove a N-MOS due to change a new MIC JACK.
23	Add a 120ohm bead L2304 and a 1000PF capacitor C2307 for EMI.
25	Add 0ohm resister R2503 and change Q2502 into unmount.
25	Add CON2502 in other to colayout with CON2501.
26	Connect not PCI_RST# but PLT_RST# to the RESET# signal of PCIE MiniCard for customer's demand.
27	Connect pin20 of MiniCard to the signal of OR conditions of WLAN_SW# and WLAN_ON# for customer's demand.
29	Change tolerance of R2918 into 1% and C2917 into 10% for the timing of EC_RST#.
29	Change WLAN_SW# into pull-up +3VSUS
30	Add 100PF capacitors C3011 and C3012 for EMI.
33	Add CON3302, RN3301, RN3302, RN3303, RN3304, RN3305 in other to colayout with CON3301.
33	Add Varistors D3304 and D3305 for EMI.
33	Change R3308 into 39ohm for the brightness of LED3301.
34	Change C3406, C3407 into 30PF in other to fit 25MHz frequency.
35	Place C3502, C3503 on the other side of L3503, L3504 for layout.
36	Change CE3602 from 100UF to 150UF in other to fit droop SPEC.
37	Change R3704, Q3705, R3708, Q3709, R3709, Q3710, R3710, Q3711, R3711, Q3711 into unmount because they don't affect the discharge circuit.
38	Change resisters R3805, R3806, R3807 into 620ohm in other to tune brightness.
41	Change the fuse F4101 into mount for customer's demand.
41	Add the colayout of JP4102 and F4102 for customer's demand.
41	Change 0ohm resister R4105 into 120ohm bead L4105 for EMI.
41	Add four Varistors D4102, D4103, D4104, D4105 and ten capacitors C4110~C4119 for EMI.
41	Chane C4103, C4104 into mount for EMI.
70	Chane R7002 into 80.6ohm for brightness.

R1.1 to R1.2

Page	Action

R1.2 to R2.0

Page	Action	Reason

PCMCIA

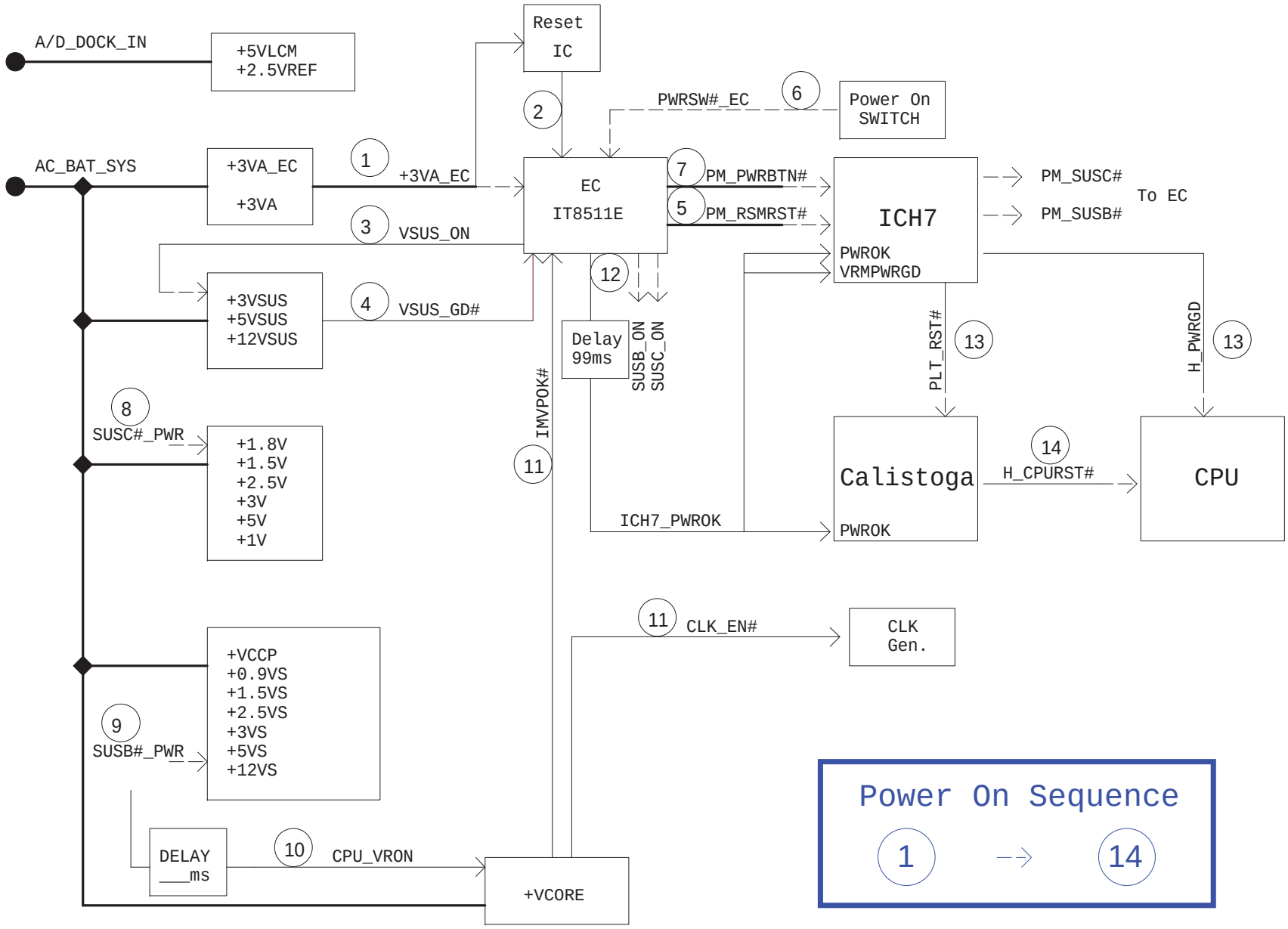
ASUSALPHA

Title : HISTORY

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 46 of 57



PCMCIA

ASUSALPHA	Title :	FLOWCHART
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 47 of 57	

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON_EC	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/	O	55	GPH2	IMVPOK#	I
37	PWM3/GPA3	BAT_LOW_BEEP(Reserved)	O	69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH_PWROK_EC	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	WATCHDOG#	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/0	155	GPI3	CHG_EN#	O
164	SMDAT0GPB4	SMDATA_BAT	I/0	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	BAT_LL#	O
6	KBRST#/GPB6	RCIN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	109	GPI7	/	
47	CLKOUT/GPC0	/	O	99	DAC0/GPJ0	CHG_FULL_LED#_EC	O
169	SMCLK1/GPC1	SMB1_CLK	I/0	100	DAC1/GPJ1	/	
170	SMDAT1/GPC2	SMB1_DAT	I/0	101	DAC2/GPJ2	INVTER_DA	O
171	GPC3	/	I	102	DAC3/GPJ3	BATSEL_2P#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	97	GPJ4	/	
175	GPC5	OP_SD#	O	98	GPJ5	/	
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I			/	
1	CK32KOUT/GPC7	/	O			/	
26	RI1#/WUI0/GPD0	PM_SUSB#	I	81	ADC0/GPK0	BAT0_AD	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I	82	ADC1/GPK1	/	
30	LPCRST#/WUI4//GPD2	PLT_RST#	I	83	ADC2/GPK2	AC_AD	I
31	ECSCI#/GPD3	ECSCI#	O	84	ADC3/GPK3	/	
41	GPD4	/		93	ADC8/GPK4	KB_ID0	I
42	GINT/GPD5	/		94	ADC9/GPK5	KB_ID0	I
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#_EC(Reserved)	I	8	GPL0	/	O
88	ADC5/GPE1	/	I	11	GPL1	/	O
89	ADC6/GPE2	/	I	12	GPL2	/	I
90	ADC7/GPE3	/	I	20	GPL3	/	O
2	PWRSW/GPE4	PWRSW#_EC	I	21	GPL4	/	
44	WUI5/GPE5	/		106	GPL5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I	107	GPL6	/	
25	CLKRUN#/WUI7/GPE7	/	O	108	GPL7	/	
110	PS2CLK0/GPF0	/		22	ECSMI#/GPM0	EXTSMI#	O
111	PS2DAT0/GPF1	/		23	PWUREQ#/GPM1	/	
114	PS2CLK1/GPF2	/	I/0	85	KSO16/GPM2	/	
115	PS2DAT1/GPF3	/	I/0	86	KSO17/GPM3	ID_EC (Reserved)	I
116	PS2CLK2/GPF4	TPAD_CLK		91	CTX/GPM4	/	
117	PS2DAT2/GPF5	TPAD_DAT		92	CRX/GPM5	/	
118	PS2CLK3/GPF6	/					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	/	I/O
AC18	GPIO07	PM_THERM#_GPIO (Reserved)	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	WLAN_SW#_ICH	I
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SC#	I
E19	GPIO13	NEWCARD_DET#	I
R4	GPIO14	BAT_LL#_ICH (Reserved)	I
E22	GPIO15	WLAN_LED#	O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STPPCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STPCPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	REQ4#/GPIO22	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	CB_SD#	O
A21	GPIO26	/	
B21	GPIO27	BTO_DEV0	I
E23	GPIO28	NEWCARD_OFF#	O
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	I/O
AC19	GPIO33/AZ_DOCK_EN#	BTO_DEV1	I
U2	GPIO34/AZ_DOCK_RST#	BTO_DEV2	I
AD21	GPIO35	/	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

Indigo: the same as T12F
Pink: different from T12F

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

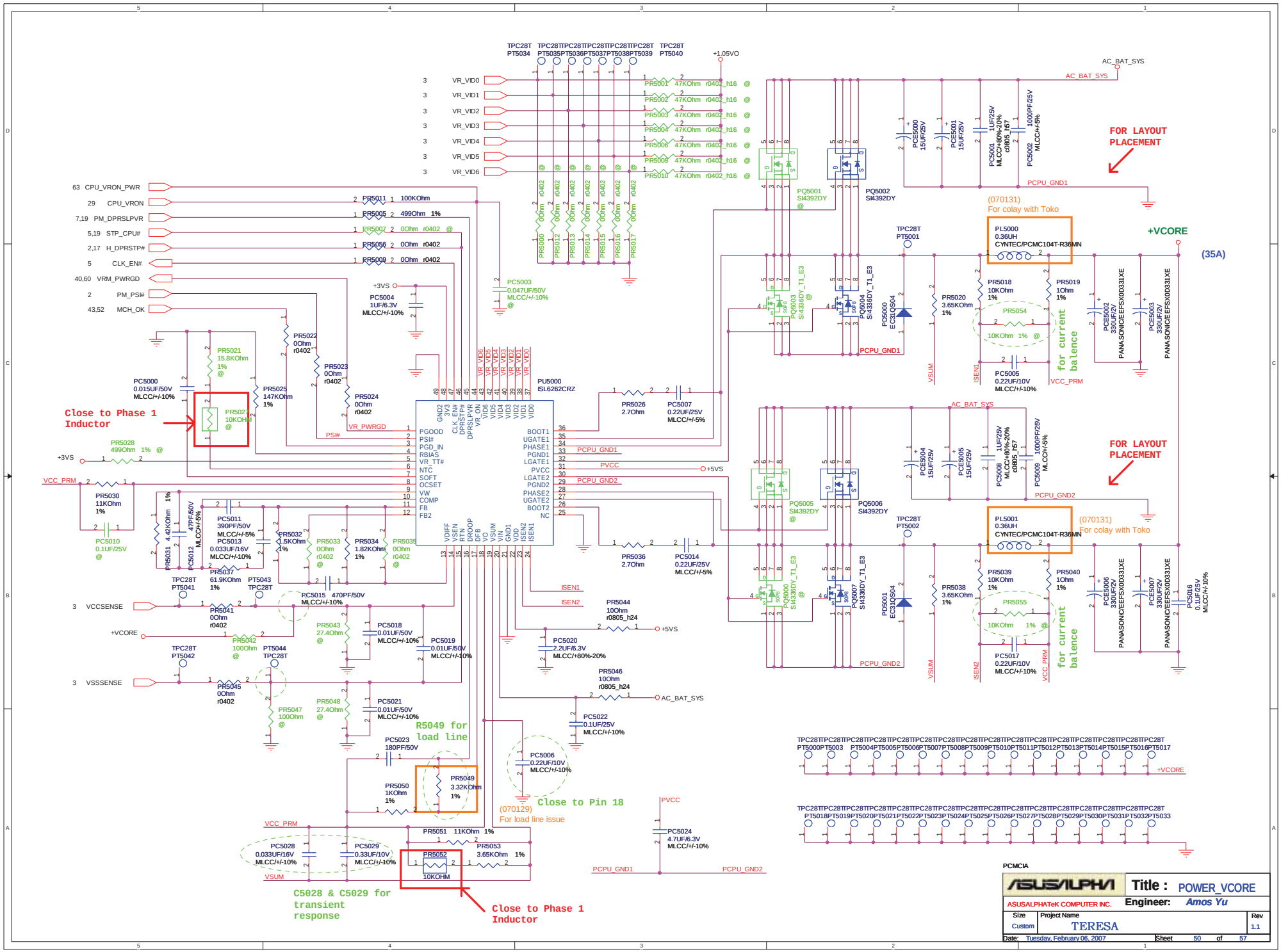
PCMCIA

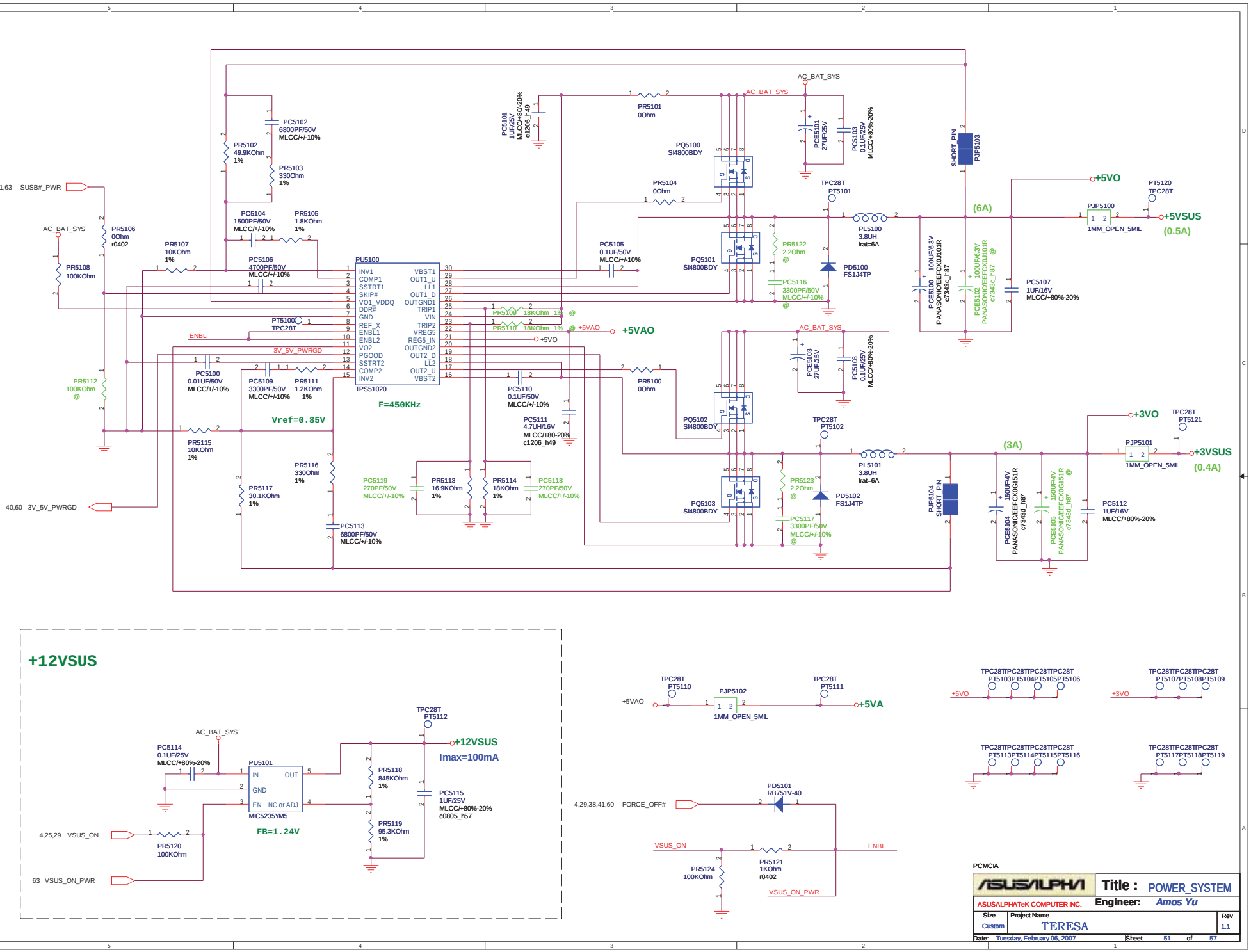
ASUSALPHA | Title : GPIO Setting

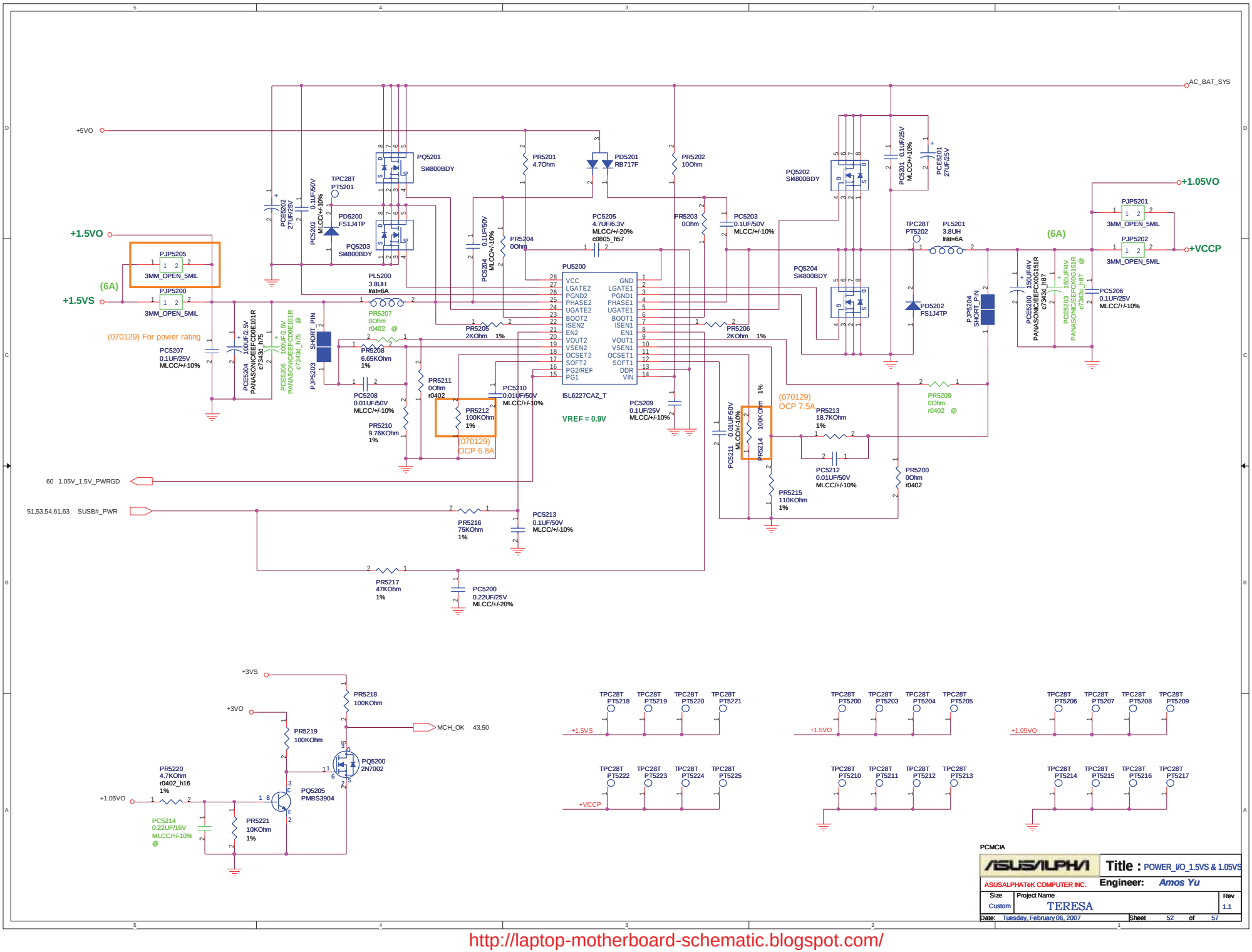
ASUSALPHATeK COMPUTER INC. | Engineer: Horng Chou

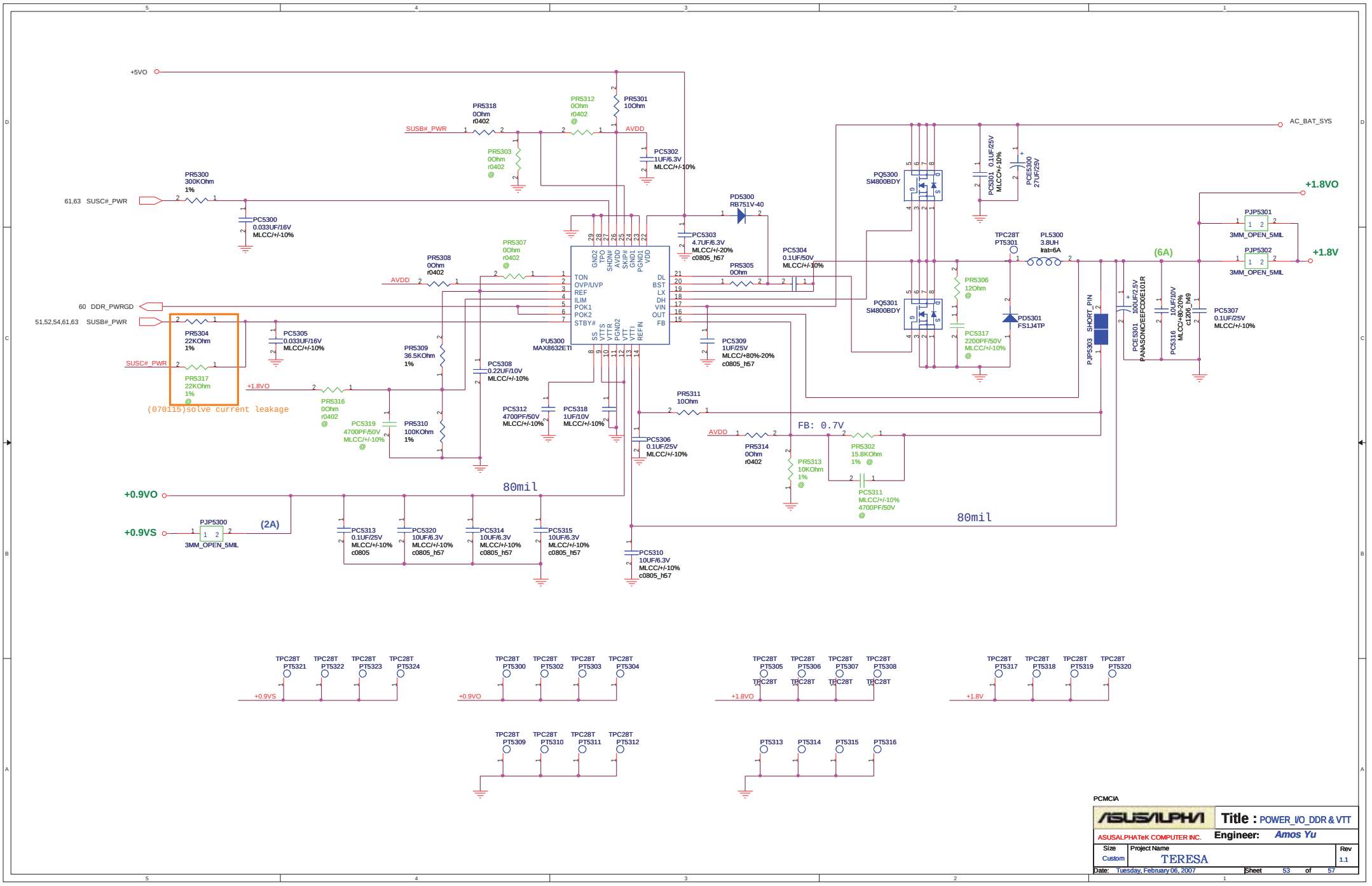
Size: Custom | Project Name: TERESA | Rev: 1.1

Date: Tuesday, February 06, 2007 | Sheet 48 of 57

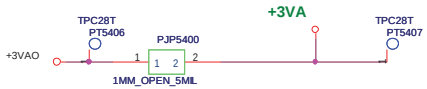


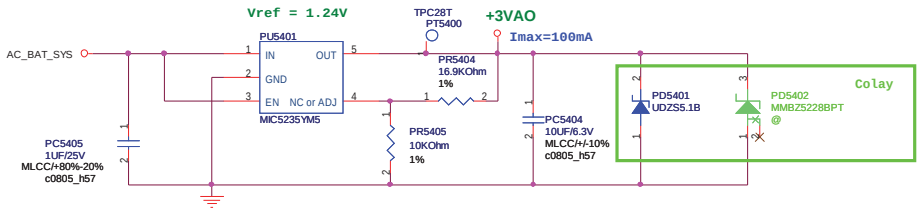




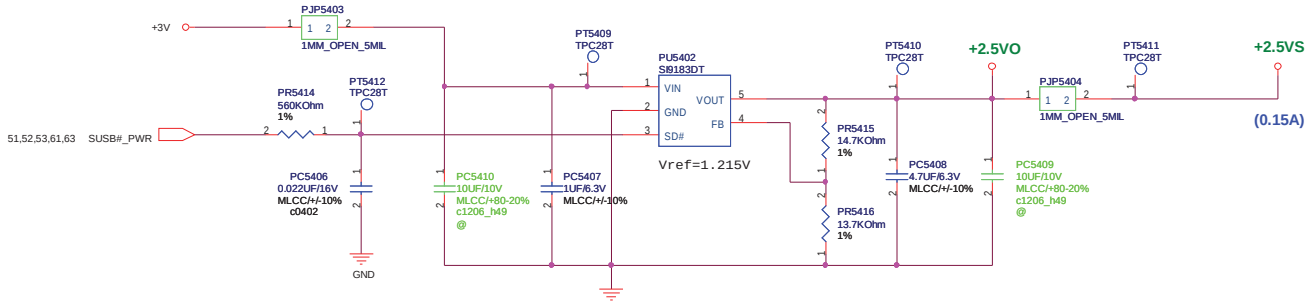


+3VA0

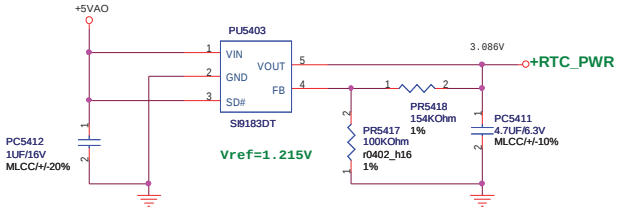




+2.5VS

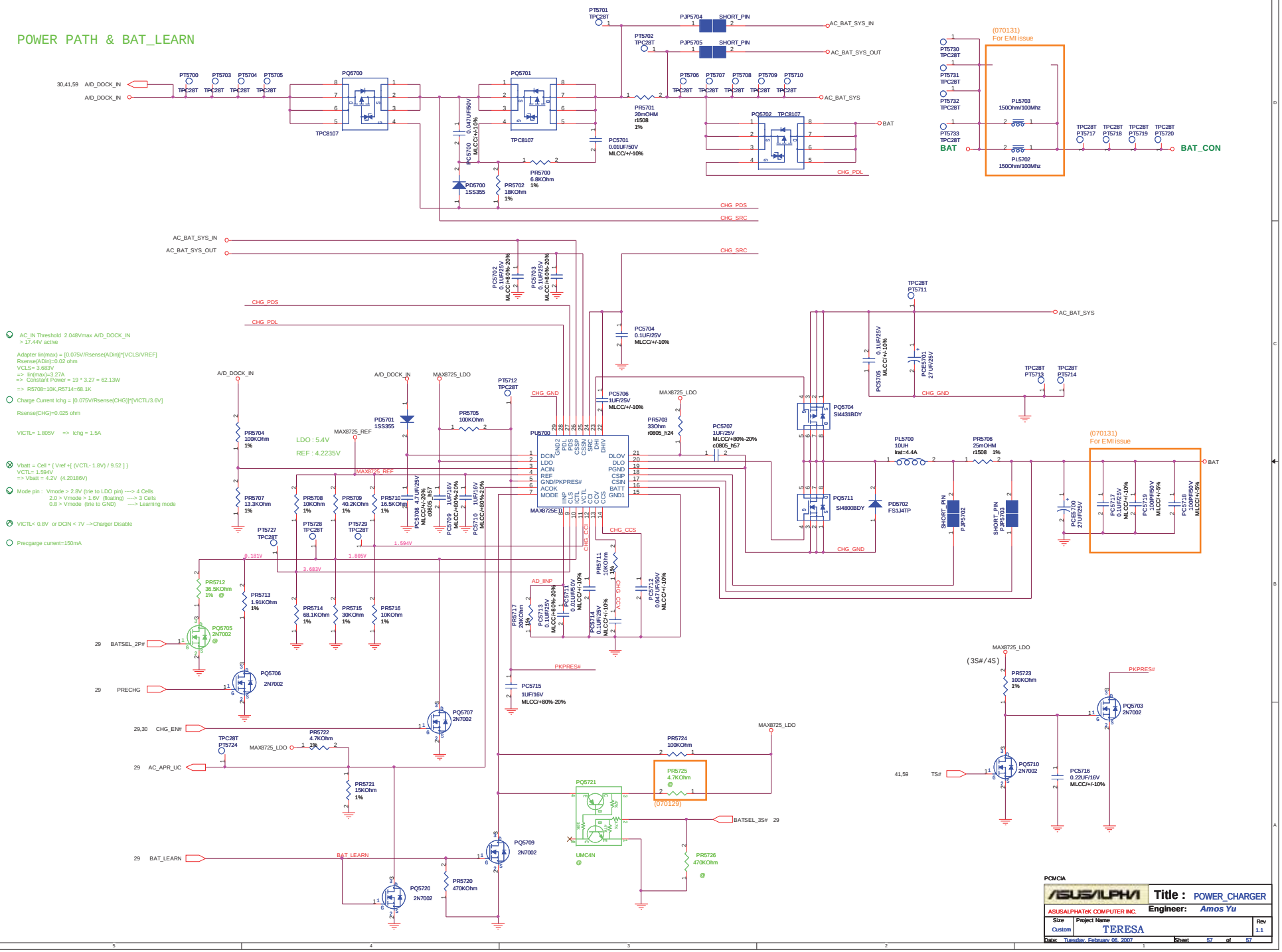


+RTC_PWR

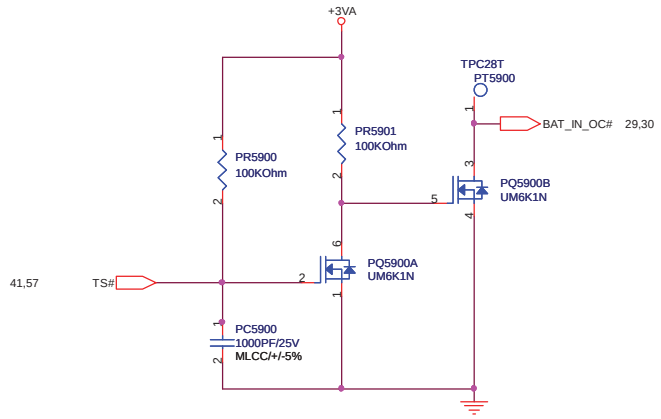


PCMCIA

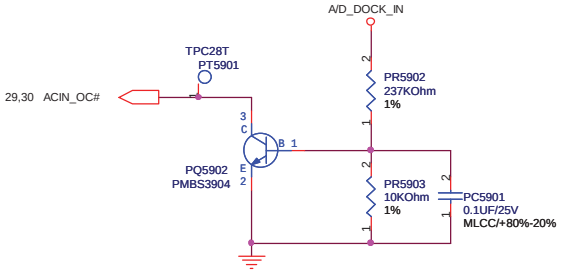
ASUSALPHA	Title : POWER_I/O_+3VA & +2.5V	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 54 of 57	



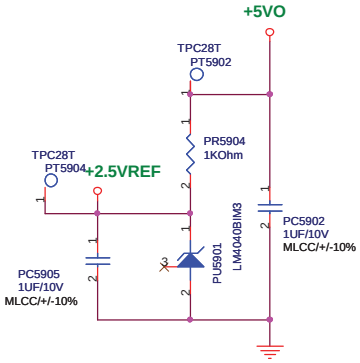
BATTERY IN DETECT



ADAPTER IN DETECT



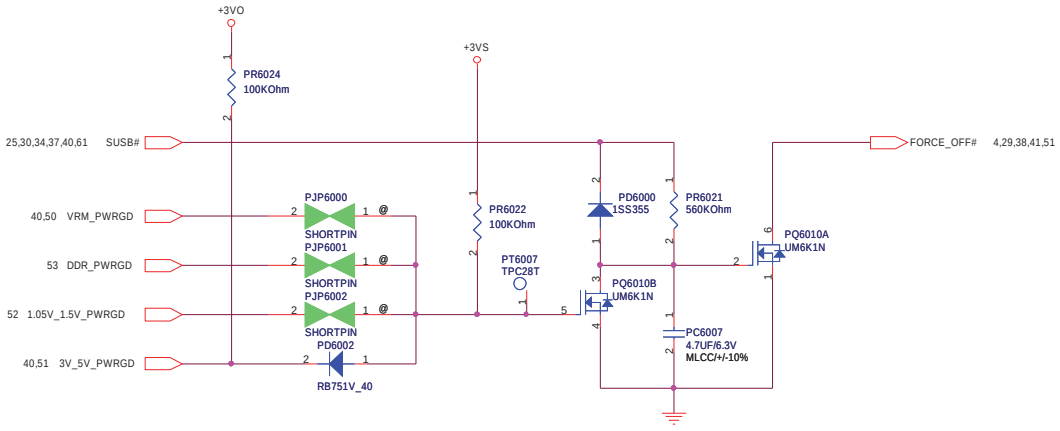
+2.5VREF



PCMCIA

ASUSALPHA	Title : POWER_DETECT	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 59 of 57	

POWER GOOD DETECTER



TPC28T PT6003 — VRM_PWRGD

TPC28T PT6004 — DDR_PWRGD

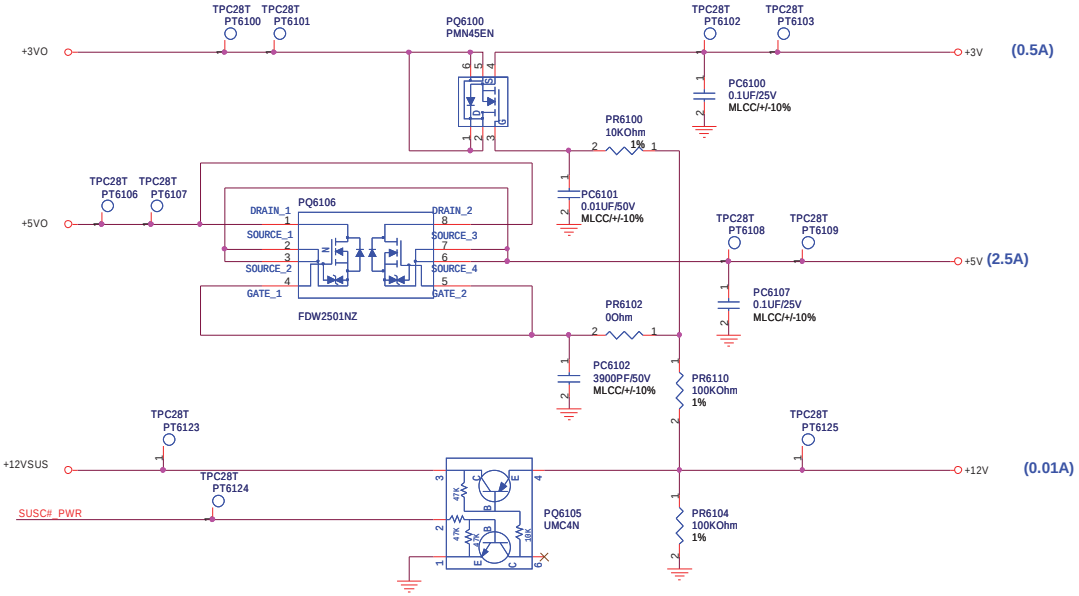
TPC28T PT6005 — 3V_5V_PWRGD

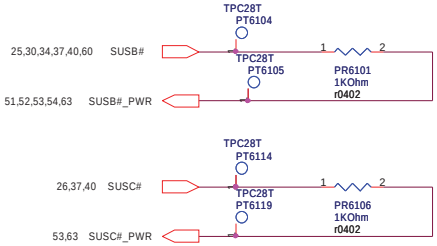
TPC28T PT6006 — 1.05V_1.5V_PWRGD

PCMCIA

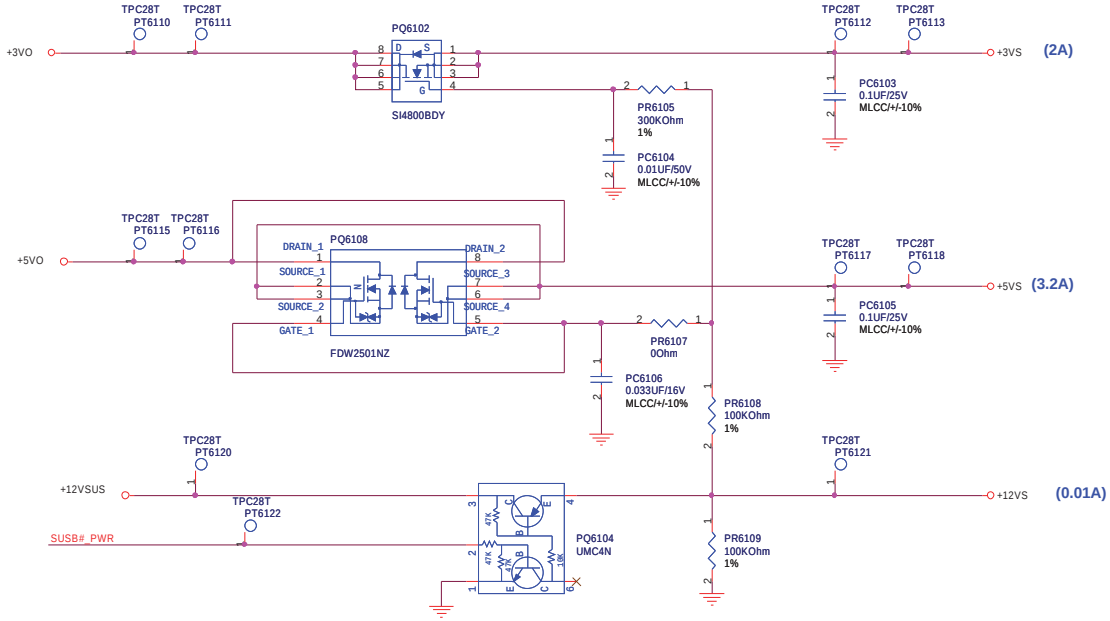
ASUSALPHA	Title : POWER_PROTECT	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 60 of 57	

SUSC#_PWR POWER



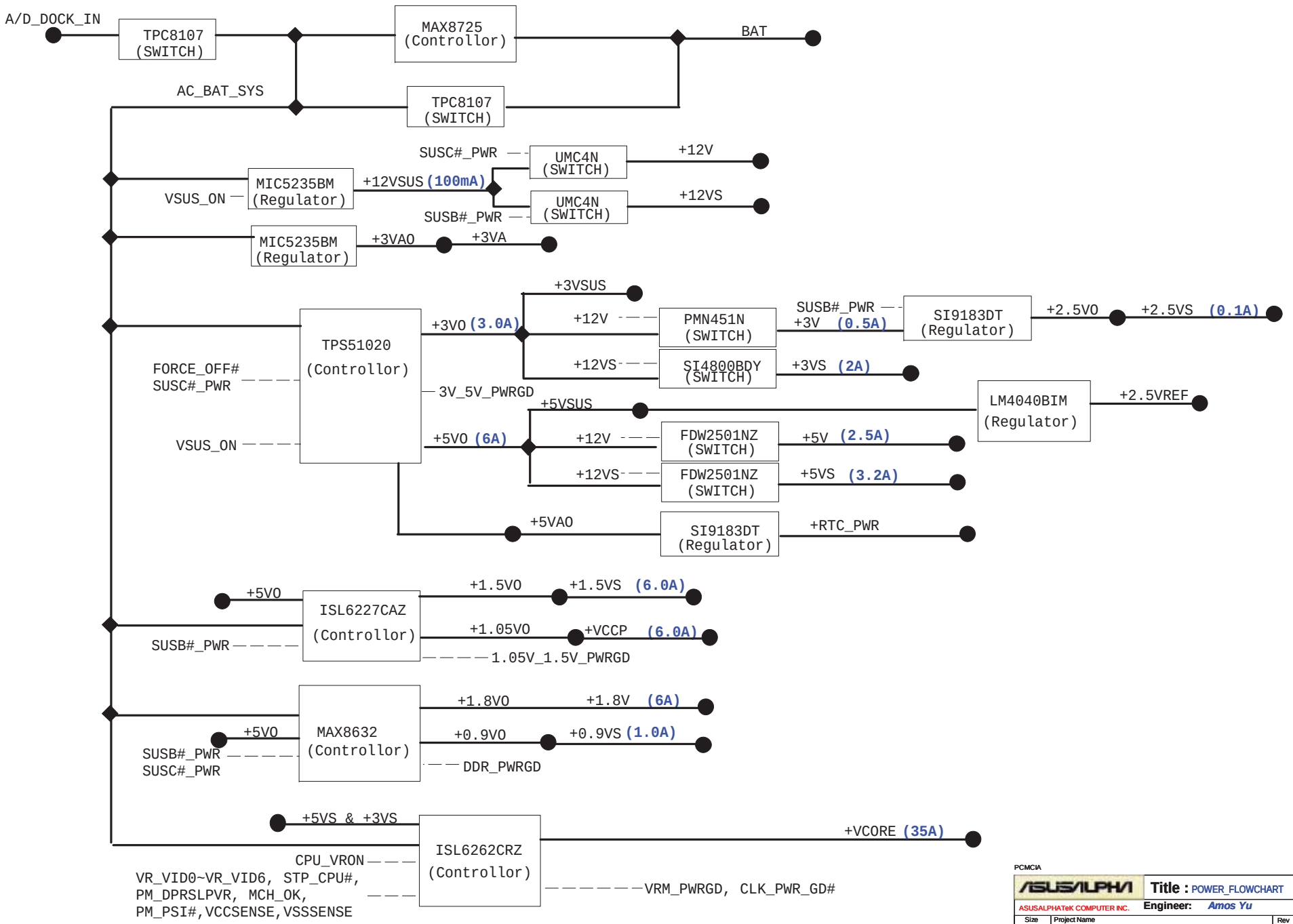


SUSB#_PWR POWER



PCMCIA

ASUSALPHA	Title : POWER_LOAD SWITCH	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 61 of 57	



AC_BAT_SYS — AC_BAT_SYS 12,41,50,51,52,53,54,57

+3VA — +3VA 4,12,22,29,37,38,40,41,54,59

+5VA — +5VA 51

+5VO — +5VO 51,52,53,59,61

+3VO — +3VO 51,52,60,61

+3VSUS — +3VSUS 18,19,20,25,29,30,34,35,40,51

+5VSUS — +5VSUS 20,30,36,51

+3V — +3V 12,18,26,37,43,44,54,61

+3VS — +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61

+12VSUS — +12VSUS 51,61

+12V — +12V 37,61

+12VS — +12VS 12,13,22,33,37,61

+5V — +5V 16,30,36,37,44,61

+5VS — +5VS 4,13,19,20,21,22,28,29,30,34,37,38,50,61

+2.5VO — +2.5VO 54

+2.5VS — +2.5VS 9,37,54

+1.8VO — +1.8VO 53

+1.8V — +1.8V 7,10,14,15,16,37,53

+VCCP — +VCCP 2,6,9,20,52

+VCCP_AGTL+ — +VCCP_AGTL+ 2,3,5,6,9

+VCCP_GMCH — +VCCP_GMCH 9,10

+VCCP_ICH — +VCCP_ICH 17,20

+0.9VS — +0.9VS 16,37,53

BAT — BAT 30,57

+2.5VREF — +2.5VREF 59

+VCORE — +VCORE 3,50

BAT_CON — BAT_CON 41,57

+RTC_PWR — +RTC_PWR 20,54

FOR POWER TEST

+3VA

PJP6300 (SGL_JUMP) — 1 | 1 2 | 2 — CPU_VRON_PWR 50

@PJP6301 (SGL_JUMP) — 1 | 1 2 | 2 — SUSB#_PWR — SUSB#_PWR 51,52,53,54,61

@PJP6302 (SGL_JUMP) — 1 | 1 2 | 2 — SUSC#_PWR — SUSC#_PWR 53,61

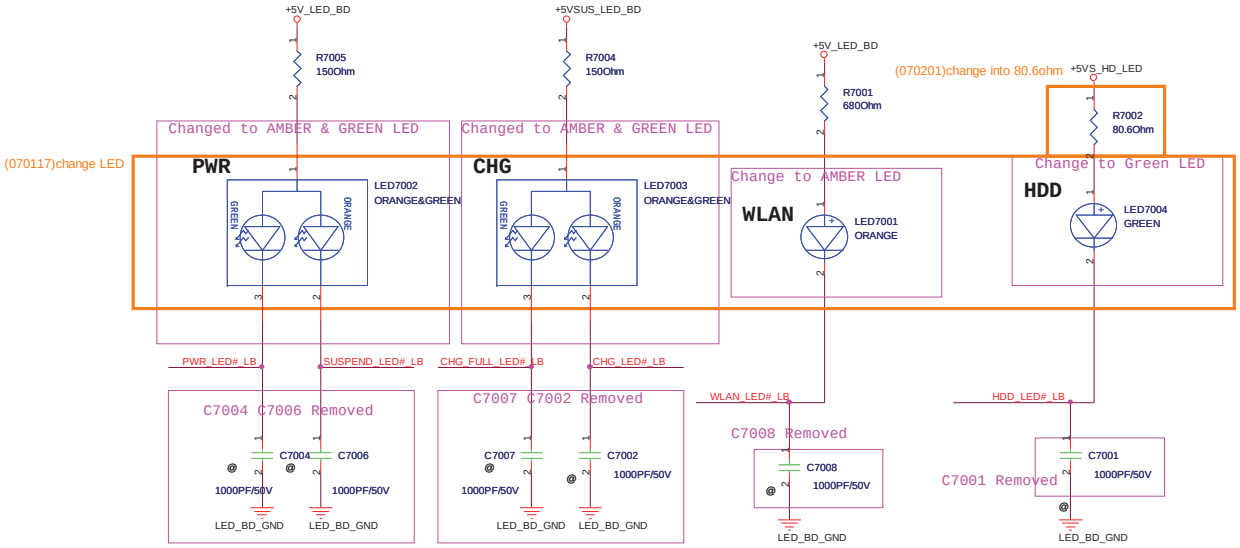
@PJP6303 (SGL_JUMP) — 1 | 1 2 | 2 — VSUS_ON_PWR — VSUS_ON_PWR 51

@

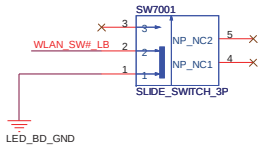
PCMCIA

ASUSALPHA	Title : POWER_SIGNAL	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 63 of 57	

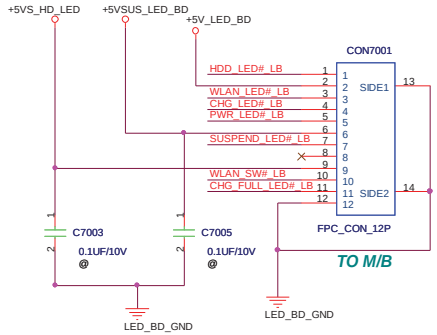
LEFT & RIGHT Button remove to TP BOARD



New added SW for Teresa

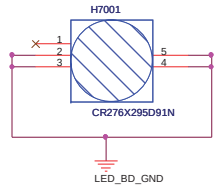


070115 Change pin define

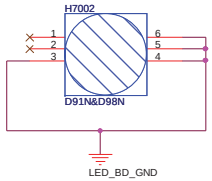


CON to T/P remove to TP BOARD

IR receive module removed



DETAIL: Q



DETAIL: S

PCMCIA

ASUSALPHA | Title : LED Board

ASUSALPHATeK COMPUTER INC. | Engineer: Potter_Huang

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 | Sheet 70 of 57

TERESA SCHEMATIC V1.0

PCMCIA

ASUSALPHA

Title : Content & History

ASUSALPHATeK COMPUTER INC.

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 99 of 57